What is not enough and What is too much! (Electrical Test)

ERAI Executive Conference 2013
Orlando, Florida
April 18-19, 2013

Sultan Ali Lilani
Technical Business Development
Integra Technologies LLC
3450 N Rock Road Building 100
Wichita, Kansas 67226

Ph 316-630-6857
Email: sultan.lilani@Integra-tech.com
Web: www.integra-tech.com

INTEGRA TECHNOLOGIES

Your Source for Test & Evaluation

Outline

- How Much Test is Really Needed
- Types of Electrical Test
- Tester Technology
- Test Costs
- Evaluating and selecting test labs
- Qualification Methods
- Q&A

Importance of Electrical Testing

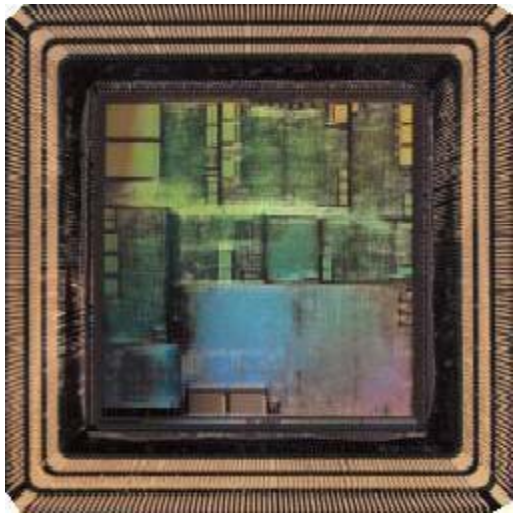
- **Effectiveness of testing has a direct correlation with the product quality**
  - All IC manufacturing requires testing (defective units are manufactured)
  - IC manufacturers are driven to reduce their testing costs
  - Manufacturers prefer to guard band and test only at room
  - Heavy use of structural testing (SCAN & BIST)
  - Some AC performance is characterized by process monitor techniques

- **Assured Avoidance of Counterfeits is dependent on a the test quality**

- **Test is often an overlooked area of evaluation users**
  - Only a few years ago was test included in Mil DSCC suitability audits
  - Lab Audits by users are rare and typically are non-technical so assessment is often minimal
  - Evaluation is needed of test techniques, technical complexity, testing equipment and integrity of test labs
  - Most who direct services of test labs have little knowledge of testing methods or technologies

- **Many classes of Counterfeit parts will pass though minimal testing**
  - At-speed functional testing is often needed to validate the device function
  - Temperature screening may be necessary to validate performance

How Much Testing is Needed



- **Risk Tradeoff**
  - Criticality of the Application
  - Source of Components
  - Costs of Testing Service
  - Amount of System Level Testing
  - Temperature needs
  - Cost of Replacement
  - Application long-term Reliability Requirements

- **Typically the OEM has the best knowledge to determine the need and type of testing**

Detection Methods

Counterfeit Type		External Visual & Phys Dim	XRF Analysis	Mark Perm	Internal Visual	Basic DC Test	Min Func Test 25C	Full Spec Extended Temps	Test & Qual
Non Functioning Devices	No Die	Possible	No	Possible	Yes	Yes	Yes	Yes	Yes
	Wrong Die Re-Marked	Possible	No	Possible	Likely	Yes	Yes	Yes	Yes
	Board Pulls	Possible	No	No	No	Possible	Likely	Yes	Yes
Functioning Devices	Failed Real Parts	No	No	No	No	Possible	Likely	Yes	Yes
	Speed up-marking	Possible	No	Possible	No	No	Possible	Yes	Yes
	Spec up-marking	Possible	No	Possible	No	No	Possible	Yes	Yes
	Temp up-range	Possible	No	Possible	No	No	No	Yes	Yes
	Pb Free Re-marked	Possible	Yes	Possible	No	No	No	No	No
	Lesser part (knock-off)	Possible	No	Possible	Possible	Possible	Possible	Likely	Yes

INTEGRA TECHNOLOGIES

Levels / Types of Electrical Test

- **Curve Tracer Testing (Not Really an Electrical Test)**
  - Level 0
  - Only validates if parts are damaged due to ESD or EOS
- **Basic DC Validation**
  (Most often provided, the lowest cost)
  - Minimal Test
- **Basic Functional Test**
  - Little more test
- **Functional Test to Specification with Parametric Testing**
  (What OEM's want)
  - Comprehensive Test
- **Upscreening needs the highest level of test coverage**
  - Temperature screening may be necessary to determine if devices are acceptable in severe environments
  - Test to Specification with Parametric Testing
  - Comprehensive functional test
  - May even need to test critical non-specified or typical parameters
- **Other Testing**
  - Qualification testing
  - Characterization Testing

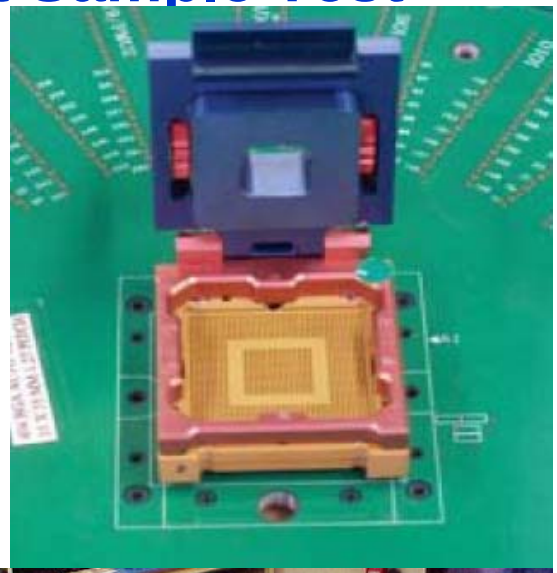
Detection Methods
Minimum Cost Sample Test

- Basic DC test
  - Pin Verification Test
  - Curve Tracer Test
  - DC only Test
  - Could be a sample Test

- IC Device
  - DC test of all pins
  - Check Continuity and Shorts on all pins
    - Make sure input/outputs and power/ground pins are in the right places
    - Make sure all power pins are correctly connected
  - Check leakage currents on input and output pins
  - Linear pins check basic pin characteristics
  - Static power supply current measurement is also possible
  - Typically will not include a functional test
- Transistor and Diodes
  - Test Basic DC device parametric values
- Capacitors and Resistors
  - Measure component value

- Will find wrong die some electrically failing parts (ESD…)

- Typical costs : $1K to 2K.



INTEGRA TECHNOLOGIES

Your Source for Test & Evaluation

Detection Methods
Basic Functional ATE Test

- **Basic Electrical test**
  - Production test of the entire lot
  - Add NRE costs if fixtures are not available
- **Simple Device**
  - Functionally test the device
  - Limited parameter measurements are performed
  - Tested at 25C
- **Complex Device**
  - Power up the device
  - Validate some limited DC measurements
    - Minimal functional test
  - Tested at 25C
- **Will find wrong die and empty parts**
  - As well as non-functional parts
- **Typical costs: NRE $2-5K and $2/unit @25C**
  - Cost dependent on unit volume and complexity

Detection Methods
Full Specification Test

- **Test the device as it is used**
  - Functional at-speed
  - Comprehensive functional testing
  - All reasonably possible patterns with memories
  - AC go-no-go of key parameters
  - Selected AC characterization measurements
  - DC measurements to the full specified limits and accuracies
  - Test all pins even with high pin count devices

- **Match the right tester to each device**
  - Tester should match the testing needs of the device
  - Use specialized engineers with test expertise in each technology commodity
    (Digital, RF, Mixed-signal, Analog, Memory, Discrete)
  - Tester optimized to the needs of each device technology

- **Testing will be similar to the original manufacturers test**

- **Full testing will find most types of counterfeit devices**

- **Add extended temp testing to assure operation over the operating range**
  - Existing test software will have minimal NRE costs
  - **Typical costs** (simple): NRE $5K-$10K @ hot/cold $2-$5 each device
  - **Typical costs** (complex) NRE $10K-$400K+ @ hot/cold $3-$10 each device

Type of Test – Production Upscreen

- **Production up-screen**
  - Critical to test parameters that would be affected by temperature
    - DC Parameters
    - At-speed testing of AC's
    - Functional coverage of all functional blocks of device
    - Even including at times typical parameters
  - Reliance on the manufacturer test
    - A good manufacturer test will find structural device defects
    - Fault grading and structural test techniques cannot be performed by test labs
    - Device modeling is proprietary to manufacturers

- **The effectiveness of up-screening rests in the quality of the test lab's electrical test program**

Type of Test - Qualification

- **Electrical test for qualification testing**
  - Majority of failures are hard functional or DC
  - Key DC's and basic functional tests are usually adequate for qualification testing
  - This will capture package related reliability failures
    - Delamination / voids
    - Moisture invasion / contamination
    - Leakage conditions

- **At-speed testing & extensive functional coverage may be required**
  - Testing to evaluate device performance over temperature
    - Plan to use the device outside the manufacture temp range
  - Die reliability evaluation requires full functional testing but not at-speed

Characterization Testing

- **Characterization is collecting data “measurements” on devices.**
- **Data can be used to evaluate device margin**
- **Over temperature characterization data can help define a device upscreen test spec limits**
- **Tester Capability**
  - Datalog Collection
  - Basic data collection on most DC parameters are standard
  - AC parameters typically are Go-No-Go “not measured”
  - Additional test development is required
    - Measurement and incremental search routines added to tests
    - Can add significant development effort
  - Nearly any parameter can be characterized
  - Schmoo plots are a graphical two dimensional representation of parameters
  - Characterization test times can be significant depending on the parameters

Electrical Subgroups

- **Traditional military testing calls out electrical subgroups**
  - Thirty years ago “DC only” testers were the primary test platform and AC tests were done using bench setups
  - Today a single test platform is capable of performing both the DC and functional testing, eliminating the need for separating these tests
  - It actually takes more development effort for a separate DC and functional version of the test program

- **DC and Functional testing is not necessarily adequate**
  - Just picking a few subgroups may not be enough test
  - Often more is needed to ensure good test coverage

- **One of the most common test descriptions is perform a**
  - Group A test (this is not a clear definition of test)

TABLE I. Group A electrical tests for classes level S and level B devices

Subgroup 1
Static tests at 25°C
Subgroup 2
Static tests at maximum rated operating temperature
Subgroup 3
Static tests at minimum rated operating temperature
Subgroup 4
Dynamic tests at 25°C
Subgroup 5
Dynamic tests at maximum rated operating temperature
Subgroup 6
Dynamic tests at minimum rated operating temperature
Subgroup 7
Functional tests at 25°C
Subgroup 8A
Functional tests at maximum rated operating temperatures
Subgroup 8B
Functional tests at minimum rated operating temperatures
Subgroup 9
Switching tests at 25°C
Subgroup 10
Switching tests at maximum rated operating temperature
Subgroup 11
Switching tests at minimum rated operating temperature

Manufacturer's Datasheet

- **Testing to 100% of the manufacturer's datasheet is often not viable**
- **Manufacturers do not test 100% of listed parameters**
  - Tests can't be performed on ATE test equipment
  - Tests are cost prohibitive to perform
  - Tests are unnecessary to validate device performance
- **Datasheet tests that can't be performed cost effectively**
  - Absolute maximum ratings / considered destructive
  - Long term drift & stability
  - Temperature controlled parameters
  - Load Conditions with low capacitance (Testers are >50pF)
  - Capacitance measurements
  - Ultra tight skew measurements
  - FMAX
  - Very small current or voltage measurements

Manufacturer's Datasheet

- **Datasheet words which may indicate testing limitations**
  - Typical parameter
  - Sampled parameter
  - For design guidance /Design Limits
  - For reference only
  - Guaranteed by design / Calculated / Ideal
  - Not 100% tested

Datasheet - LM35D Temperature Sensor

Parameter	Conditions Tmax= 125 C Tmin= -55 C	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy,	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
LM35, LM35C	T_A=−10°C	±0.5			±0.5		±1.5	°C
(Note 7)	T_A=T_{MAX}	±0.8	±1.5		±0.8		±1.5	°C
	T_A=T_{MIN}	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D	T_A=+25°C				±0.6	±1.5		°C
(Note 7)	T_A=T_{MAX}				±0.9		±2.0	°C
	T_A=T_{MIN}				±0.9		±2.0	°C
Nonlinearity (Note 8)	T_{MIN}≤T_A≤T_{MAX}	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	T_{MIN}≤T_A≤T_{MAX}	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
(Note 3) 0≤I_L≤1 mA	T_{MIN}≤T_A≤T_{MAX}	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
(Note 3)	4V≤V_S≤30V	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current	V_S=+5V, +25°C	56	80		56	80		µA
(Note 9)	V_S=+5V	**105**		**158**	**91**		**138**	µA
	V_S=+30V, +25°C	56.2	82		56.2	82		µA
	V_S=+30V	**105.5**		**161**	**91.5**		**141**	µA

Note 4: Tested Limits are guaranteed and 100% tested in production.

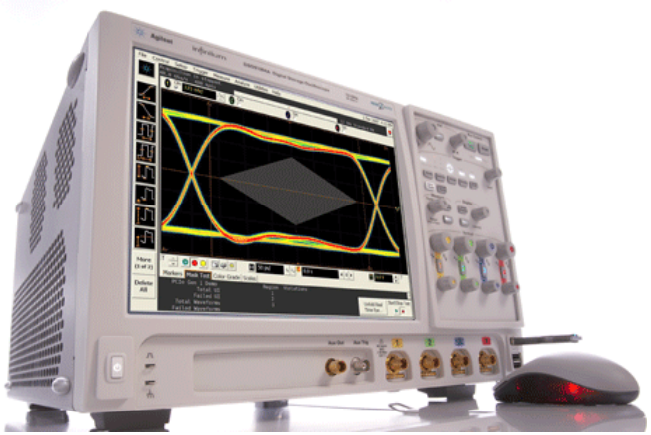
Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

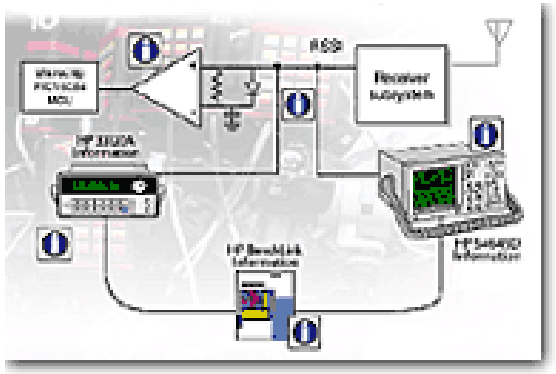
Testing Exceptions: Nonlinearity and Sensor Gain

Would require serialized data collection at multiple temperatures & data calculations to characterize the parameter

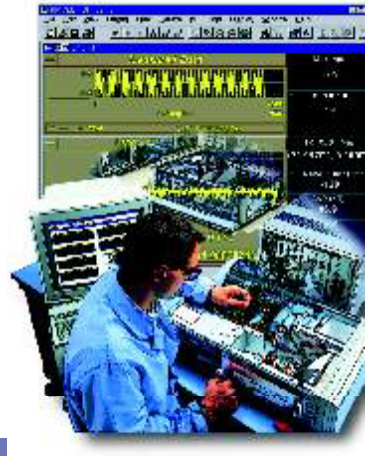
Test Equipment Used



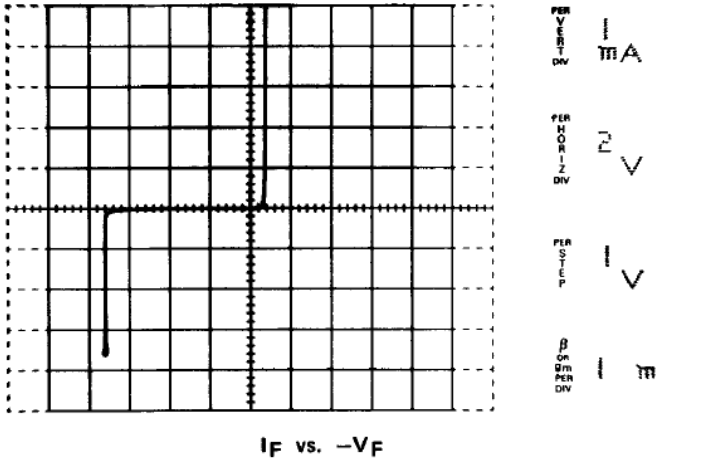
Bench Equipment
Methods of Minimal Testing



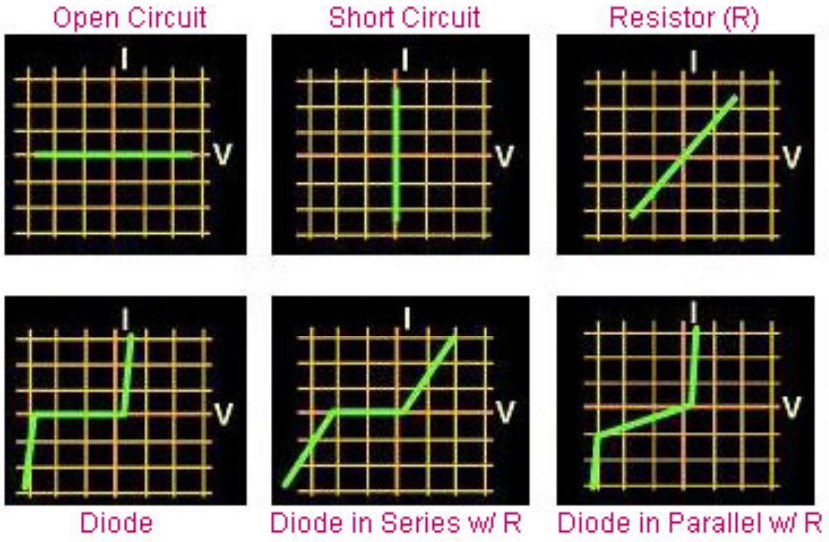
- **Minimal Capital Investment costs**
  - $10K to $100K (lab setup)
- **Basic Bench Equipment**
  - Power Supply
  - Curve Tracer
  - Multi-meter
- **Extended Bench Equipment (add some functional Test)**
  - Function Generator
  - Oscilloscope
  - Impedance Analyzer
- **Labor Intensive Testing**
- **Reasonable Effective for minimal complexity devices**



Basic Bench Equipment
Curve Tracer (V-I Curve)



I_F vs. $-V_F$



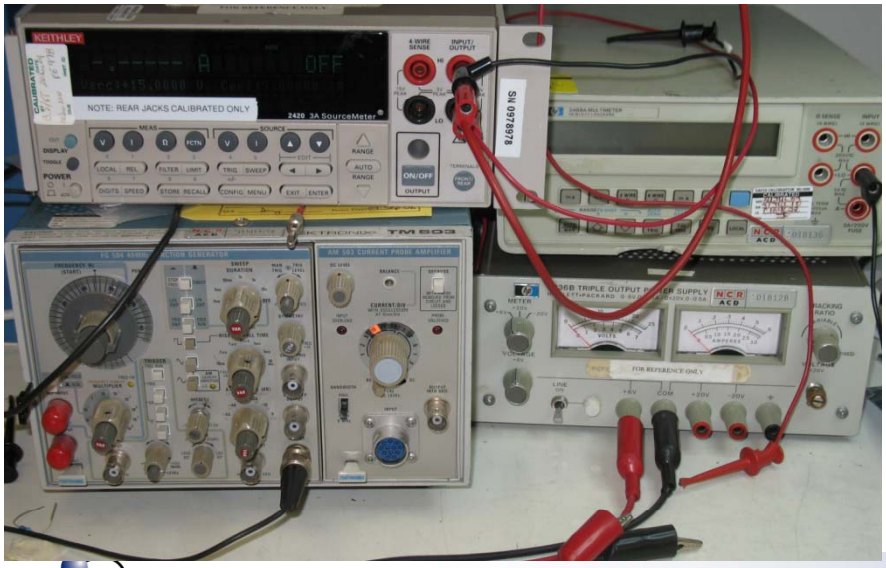
From: siliconfareast.com

INTEGRA TECHNOLOGIES

Your Source for Test & Evaluation

Basic Functional Bench Equipment

- Scope
- Power Supplies
- Function Generator
- Multi-meter
- Impedance Analyzer



INTEGRA TECHNOLOGIES

Your Source for Test & Evaluation

Complex Computer Controlled RF Bench Setup

INTEGRA TECHNOLOGIES

Automatic Test Equipment (ATE)

- **What is an ATE**
  - Tester (typical name)
  - Computerized Controlled Bench
  - Testers have the same basic capabilities as a bench
    - Voltage
    - Current
    - Timing
  - Add automation and flexibility
    - Equipment controlled by computer software
    - Quickly change configuration & Test setup
    - Great flexibility switchable resources

Typical Modern ATE

- **Fully Custom System**
  - Not bench equipment stacked up
  - Custom boards to implement testing functions
  - Tight integration of computer an hardware
  - Customized computer language
  - Optimized for fast test times not low system cost
- **Computer**
  - PC, Sun or custom
  - Typically as fast as possible for technology of the time
  - Fast interface to tester (typically custom)
- **Main Frame**
  - Power Supplies
  - Older systems had memory & control functions
- **Test Head**
  - Precision resources (voltage, current & timing)
  - Pin Cards (digital pins 4, 8 … 64 each)
    - Vector pattern generation
  - Analog resources (DC, source/capture waveforms)
  - Power Supply Connection
  - Movable to interface to handling equipment with alignment
- **Load Board**
  - Mounts on Test Head
  - Typically pogo pin connection
  - Device interface DUT (Device Under Test)
  - Device Test Socket (sometimes multi-site)
  - Handler Interface

Why So Many Types of Testers

General Test Methodology
Match the Tester to the Device

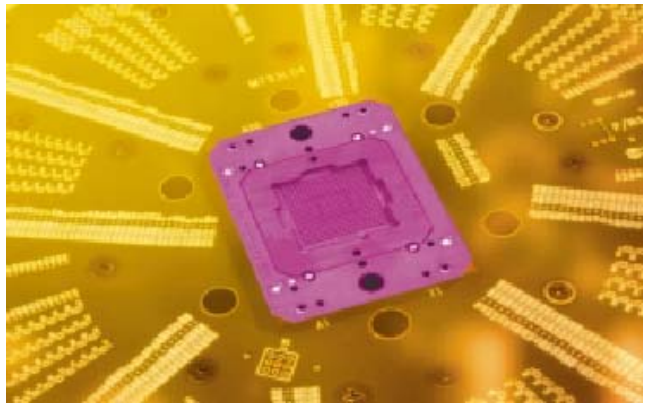
- **No single tester can effectively test all device types**
- **Effective testing matches the tester to the device requirements**
  - Tester optimized to the needs of each device technology
  - Highest test capability with lowest costs
- **Specialized engineers for each tester and technology**
  - No engineer can be an expert in every area of test
  - Manufacturer engineers specialize in specific test technologies
- **Look for a lab with broad device technology capability**
  - Digital, Linear, RF, Memory, Mixed Signal, uP, FPGA …
  - Most Labs can't bid on all device types (need multiple labs)
- **Complex devices drive the need for very high capability testers**

  500+ pins

  >100Mhz & >6GHz RF

  >14 bit D/A & A/D resources

Tester Types



- **Testers optimized to device technologies**
- **Major Classes of Devices**
  - Digital
  - Memory
  - RF
  - Analog
  - Mixed Signal
- **Each class of devices are further divided by performance and needs**
  - Speed (frequency)
  - Low / High Current & Voltage
  - Mixed technology needs
- **No single tester made today can adequately test every device**
  - But they are more flexible than in the past

Memory Testing Issues

- **High speed memories are very challenging to test**
  - High cost of test equipment
  - Fast switching times & high frequencies
  - Transmission line effects (impedance mismatch reflections)
  - Ground bounce
- **Extended pattern coverage can drive test times and costs up significantly**
- **Speed of the device can be derated to lower speed grades as elevated temperature ranges extend**
- **Ongoing production upscreen testing is important**
  - Frequent of die shrinks
  - Limited availability of industrial grade devices
  - High usage content per application
- **Memory technology pushes technology limits leading to more quality and reliability issues**
- **Specification limits typically have minimal margin**
  - Testing at hot and cold temperature extremes can push the device outside the specification limits
  - Characterization is recommended at temperature extremes

Test Methodology
Digital Devices & Microprocessors

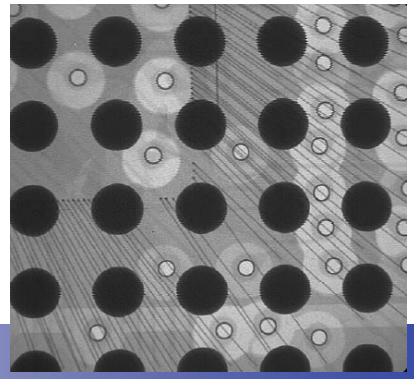
- **Testing performed to verify the functionality of the device**
  - Test at full application frequency
  - Test Key DC and functional AC parameters
    - AC parameters that access the device's performance such as frequency testing, input setup/hold times and output delay measurements
  - Generally every functional block of the device should be exercised
  - All instruction groups are exercised
- **Requires an engineer with extensive experience specific to microprocessor test software development**
- **Required tester capability**
  - External Frequency = 100/400+ MHz
  - Pin count = >500 pins
  - Output impedance mismatch damping
  - DC measurement (PMU per pin)
  - Loadboard trace length De-skew
  - High Accuracy +/-200ps

Test Methodology
FPGA – Programmable Logic

- **FPGAs come in two major types**
  - One-time Programmable
  - Re-programmable (EPROM/FLASH/RAM based)
- **Each type has a unique test strategy**
  - **One-time programmable** (Actel, Quicklogic)
    - Test blank (limited DC's & very minimal test value)
    - Program device with user code (test to the loaded code)
      - Test like an ASIC and every design needs a new test program
      - Acugen S/W can generate fault graded test vectors
  - **Re-programmable** (Altera/Cypress/Xilinx/Vantis)
    - Test developed independent of customer design
    - Develop a comprehensive but testable design
    - Use in-house tools (purchase from manufacturer)
    - Create the test vectors and configuration vectors for tester
    - Functional at speed testing (using design modeling not spec)
    - Datasheet AC specs are internal FPGA performance characteristics
- **Required tester capability**
  - Frequency 100+ MHz
  - Pin count 512 pins or more

Microprocessor / FPGA Testing Issues

- **High frequency microprocessors are challenging to test**
  - High current consumption causes ground bounce effects
  - Transmission line effects (impedance mismatch reflections)
  - Device complexity (pipelining, cache, instruction sets)
- **Technology pushes technology limits leading to more quality and reliability issues**
- **Determining the test limits is a key issue**
  - The datasheet specification generally references internal gate delays and not the programmed device performance
  - AC testing specs must be generated by device modeling
- **FPGA Testing to a user design can be difficult**
  - Generally, end user designs are developed without test considerations
  - The design may have buried sequential logic limiting effective test
  - AC test limits determined by models or trial and error
- **Die sizes and packages can be very large**
  - High fixture costs
  - High tester costs
  - Complex test development



Test Methodology
RF

- **Testing performed to verify the functionality of the device**
  - Datasheets often don't give clear test limits
  - Test limits are at times derated for fixture limitations
  - Customer RF engineers can help assure application functional coverage
- **Experienced engineering staff with RF is a must**
  - RF testing is altogether different that other test disciplines
- **The types of tests that can be performed include**
  - Noise figure
  - Third order intercept
  - 1db compression point
  - Return loss (input and output)
  - Gain and phase
  - S parameter measurements
  - Operating and standby current
  - Other basic bench measurable DC and RF measurements
- **Required tester capability**
  - Wide frequency range 1 MHz to 20 Ghz+
  - Multiple RF sources
  - Digitizer
  - Spectrum analyzer
  - Network Analyzer
  - Power meters

RF Testing Issues

- **Limits may need to be defined based on test characterization**
  - Results in changes to limits over time
  - Fixture limitations / Correlation factors
- **Parameters required for critical device functionality may not be listed in the datasheet**
  - Recommendations will have to be made by an RF test expert
- **Device fixture requirements are a major cost driver**
- **Limited test lab options available**
- **Parameters may very dramatically over temperature ranges**
- **Lot to lot yield variations are common**

What Should We Do To Minimize Cost Schedule and Not Over-Test

Understanding Customer Requirements and Creating a Test Plan

Step 1: Understand Customer's Application & Requirement

- May be their application is not so complicated
  - EX: Space application within command capsule vs. outside the capsule have different requirements
  - Hand held commercial tool application vs. command module application for space craft
- Man be they are not using the entire chip
  - Nobody uses 100% of the FPGA or Microc0ntrollwe available functionality
- May be they are not needing to test to entire temperature range
- May be they have a down stream functional test at card or box level

Step 2: Understand Customer's Schedule

- Not everything is expedite

Step 2: Create A Test Plan That meet the Customer Requirements

Create a Test Plan That Meets Customer's Requirements

- It is imperative that the test plan takes into consideration the reason for electrical testing:
  - This is not upscreening; rather it is counterfeit validation. Not everything per datasheet may need to be tested.
- Choose level of testing
  - In some cases; level 1 (DC at 25C) may be adequate:
    - Application is not critical (ex: hand held consumer application)
    - Enough data is available to believe that the parts may not be counterfeit
    - but not 100% sure
    - Adequate upstream board or system level testing is available
    - Good test plan will have some level of output DC check. It means known good
    - data should be input to get a good output
  - In some cases, level 2 (DC plus functional testing) may be adequate
    - Application is somewhat critical (ex: industrial communication device)
    - Enough data is available to believe that the parts may not be counterfeit
    - but not 100% sure
    - Adequate upstream board or system level testing is not available
    - Good test plan will have some level of output DC check plus some basic
    - functionality tested. Test one or two key functionality of the device.
  - etc.

Recommended Test Methodology

- **Test the device as it is used**
  - Functional at-speed
    - Application speed at a minimum may not need spec speed
    - Test frequency is a major tester cost driver
  - Comprehensive functional testing
    - Test all device functionality
    - Fault grading is not possible
      - Only the manufacturer has device modeling capability
  - Test key AC parameters
    - Key parameters are usually referenced to device clocks
      - Propagation delay
      - Setup and hold times
      - Extra parameters are often listed for designer reference
    - Use go-no-go testing to cover most AC parameters
      - Tested over the entire functional pattern
    - Selected AC characterization measurements can be made
  - DC measurements to the full specified limits
    - Attempt to test 25C parameters at extended temperatures
    - Limit adjustments may be required after testing
  - Select the appropriate tester
    - No one tester can effectively test all technologies

Optimal Microprocessor Test Example

- **The basic approach is to use the test system to set up the basic ability to read/write the microprocessor (uP) and then use an commercially available uP emulator or simulator to generate all the device responses.**
- **The customer's actual system level application code is then loaded into the emulator and also loaded into the test program.**
- **The test program then learns the device responses from the emulator/simulator and stores them in the test program.**
- **This technique still requires competent test engineers and capable test equipment, but with those two ingredients, the test development cost can be reduced by up to 50% and the test development time can be reduced by up to one-third. Be sure the test equipment being used is capable!!**

Optimal Memory Testing Example

- **High speed memories are very challenging to test**
  - High cost of test equipment
  - Fast switching times & high frequencies
  - Transmission line effects (impedance mismatch reflections)
  - Ground bounce
- **Extended pattern coverage can drive test times and costs up significantly**
- **Speed of the device can be derated to lower speed grades as elevated temperature ranges extend**
- **Memory technology pushes technology limits leading to more quality and reliability issues**
- **Specification limits typically have minimal margin**
  - Testing at hot and cold temperature extremes can push the device outside the specification limits
  - Characterization is recommended at temperature extremes
- **Choosing a capable test system is very important!**

Test Cost Drivers

Software Development

- **As IC's have increased in complexity, the S/W NRE costs have also increased**
- **It is difficult to find a test lab with the S/W you need "on-the-shelf" and ready to go when you need it**
- **If a lab has a version of the S/W you need, a complete review of parameters tested is a must prior to committing**
- **New S/W NRE's are usually composed of three parts:**
  - Engineering
  - Tester
  - Load board and socket costs

Test Cost Drivers

- **Software Development NRE**
  - Complexity of device → Costs
  - Engineering rates
    $100/hr to $200/hr
  - Tester charges
    $50/hr to $300/hr
  - Loadboard & socket NRE
    $300 to $10,000

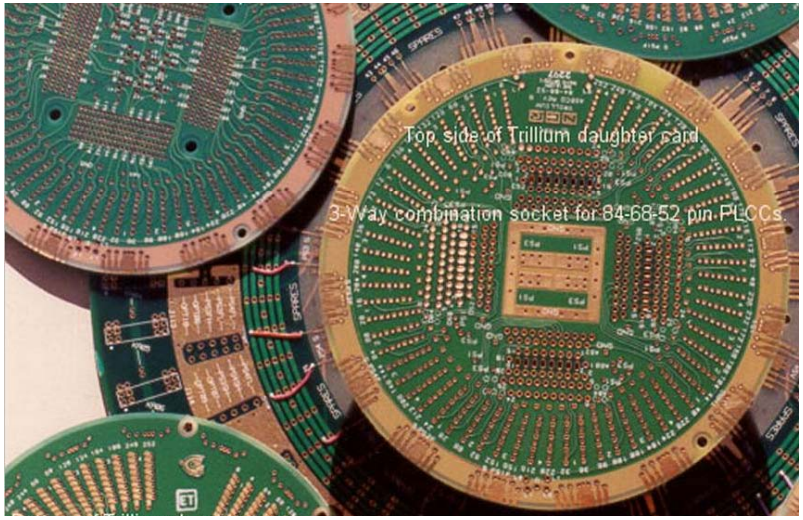
- **Production Test**
  - Volume
    - >1000pc lots (automated handling)
  - Data Collection
    - Adder for data more for serialization
  - Test flow
    - Hot & Cold tests are more costly

Loadboard / Hardware costs

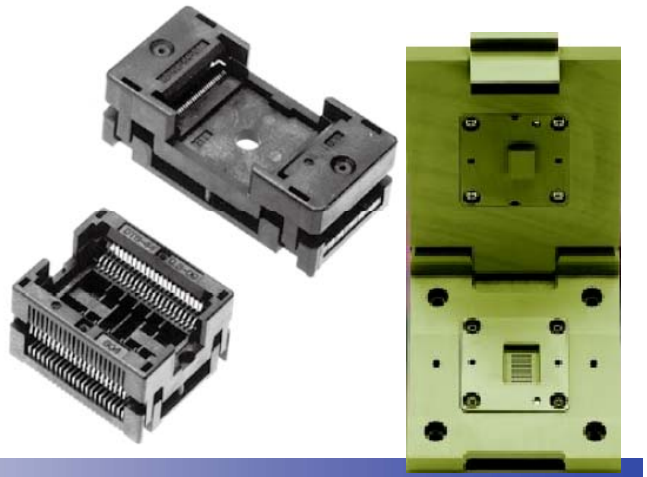
- **Loadboards**
  - Originally tester interface boards had device loads on them.
  - Now testers implement this function internally
  - The name stuck

- **DUT Boards**
  - Smaller low cost board piggyback on top of a larger loadboard
  - Can save significant cost
  - Increases setup issues and degrades signal quality

- **Board Costs**
  - Low pin count hand wired DUT Boards ($100 to $800)
  - Semi custom loadboards boards for typical packages $1500
  - Full custom boards (high pinout or complex hardware) $10K



- **Socket Costs**
  - Basic off the shelf molded burn-in type socket ($20 to $500)
    - Very limited numbers of test insertions (100 to 10K typically)
    - Poor electrical performance
  - Custom made production sockets ($1500 to $5000)
    - Higher test insertions and reparable (>100K insertions typically)
    - Electrical performance needed for high speeds, accuracy or RF testing



INTEGRA TECHNOLOGIES

High Volume Throughput (Parts Per Hour)
Semiconductor Manufacturer Handler Example

Single Site
Test time = 10 sec.
n = 1
Index = 0.3 sec.
Utilization = 0.85

$$\text{PPH} = \frac{3600 * 1 * 0.85}{10 + 0.3}$$

PPH = 297
@$100/hr
$0.34/device

Dual Site
Test time = 13 sec.
n = 2
Index = 0.35 sec.
Utilization = 0.85

$$\text{PPH} = \frac{3600 * 2 * 0.85}{13 + 0.35}$$

PPH = 458
@$100/hr
$0.22/device

INTEGRA TECHNOLOGIES

Low Volume Production Test
Cost Drivers

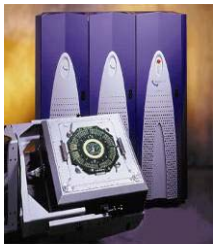
- **Cost Attributes**
  - Setup time can be significant (>1 hour)
  - Opinions regarding the definition of high and low volumes vary from lab to lab
  - Small lot sizes are not cost effective and result in low volume screening
- **Volume**
  - High volume can drive auto handler testing which greatly reduces costs
  - Low volume makes NRE handler kit costs prohibitive and drives hand test in most cases
- **Data Collection**
  - Attributes Only (called Go/No/Go or pass/fail) is the least costly
  - Datalog collection increases costs
    - All devices datalogged or “failing devices only” impacts cost
  - Serialized “datalogs with deltas” is the most expensive option
- **Test Flow**
  - Number of processing steps impacts costs
  - Electrical test temperature
    - Added soak time at temperature (1 to 5 min)
    - Cold is most costly, followed by hot and then room

Questions & Answers

Integra Test Engineering
Summary

- Test Facilities in Kansas and California
  - 37k sq ft (KS), 3k sq ft (CA)
- 26 Year History as a Testing Lab
- 24 Hours/Day x 7 Days/Week Operations
- 160 Employees, 23 Test Engineers & 36 Testers
- Broad tester and test technology capabilities
  - Memory, Digital, Linear, Mixed Signal, RF, FPGA
- Engineering expertise in every technology
  - Greater than 10,000 test programs developed locally
- 165 Active Customers Mil/Space & Semi-manufacturer
- Operations are ISO-9001, AS9100, ITAR & DSCC Registered
- On-Time Delivery Performance of 96%
- Customer Satisfaction Rating of 98%







INTEGRA TECHNOLOGIES