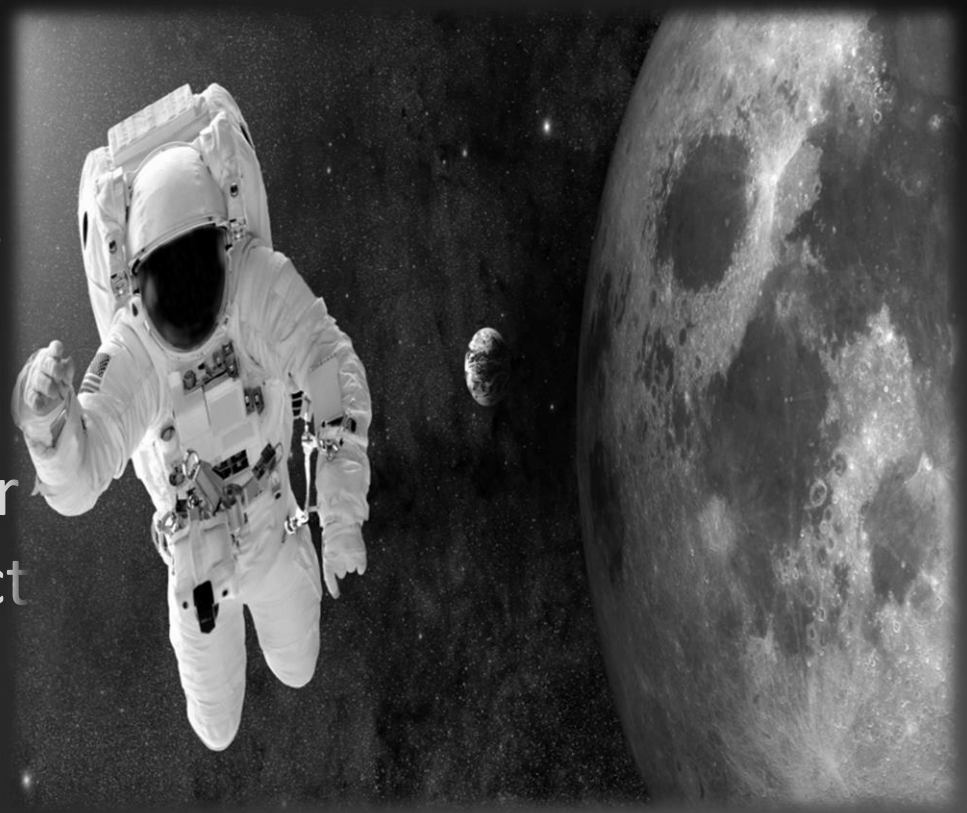
RMV TECHNOLOGY GROUP LLC

A NASA Industry Partner

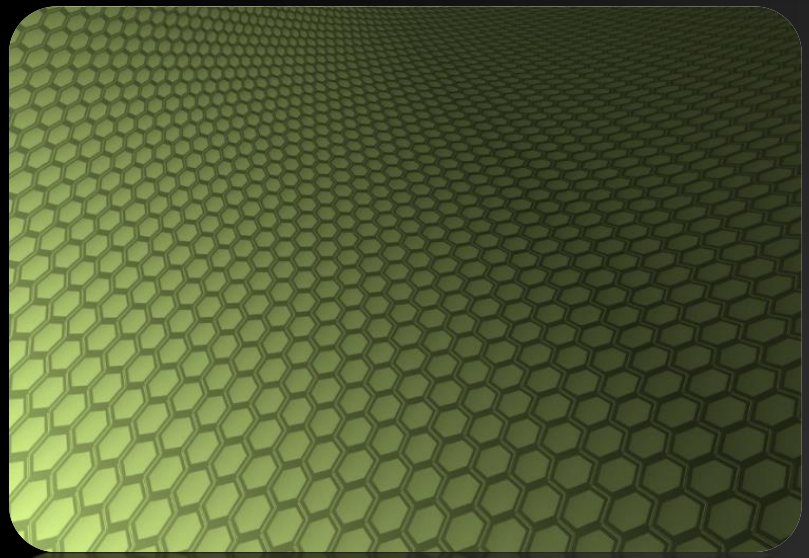
Initial Material Qualification must be Reinforced with Periodic Verification Testing Throughout the Product Life Cycle Due To Supplier Noncompliance & Suspect Counterfeiting!



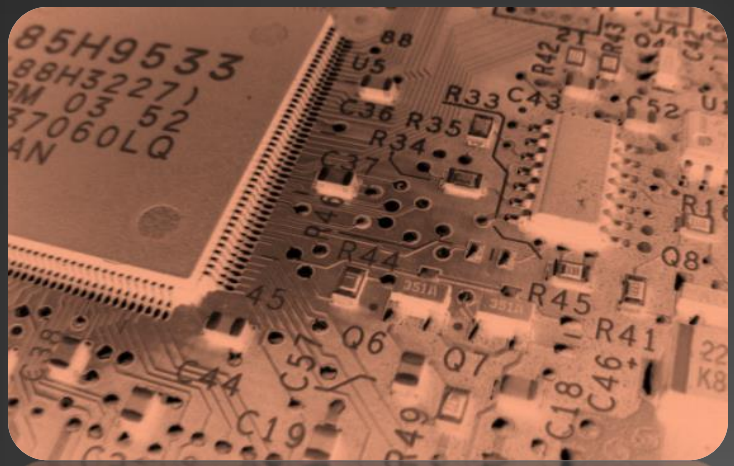
ERAI: 19 April 2013 Time: 12:00 PM to 12:30 PM

Suspect Counterfeiting Transcends…

Equipment

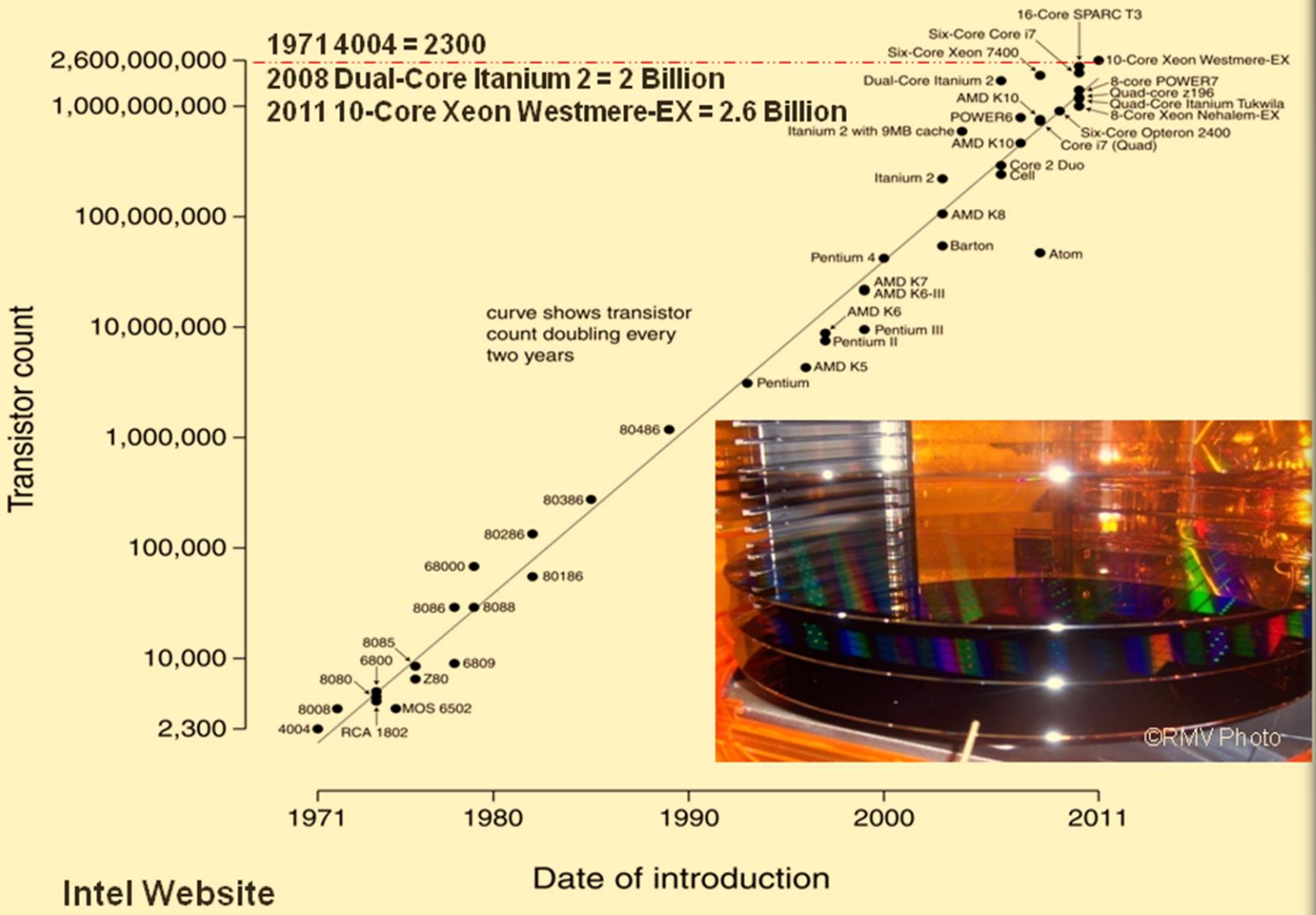


Materials



Components

Microprocessor Transistor Counts 1971-2011 & Moore's Law



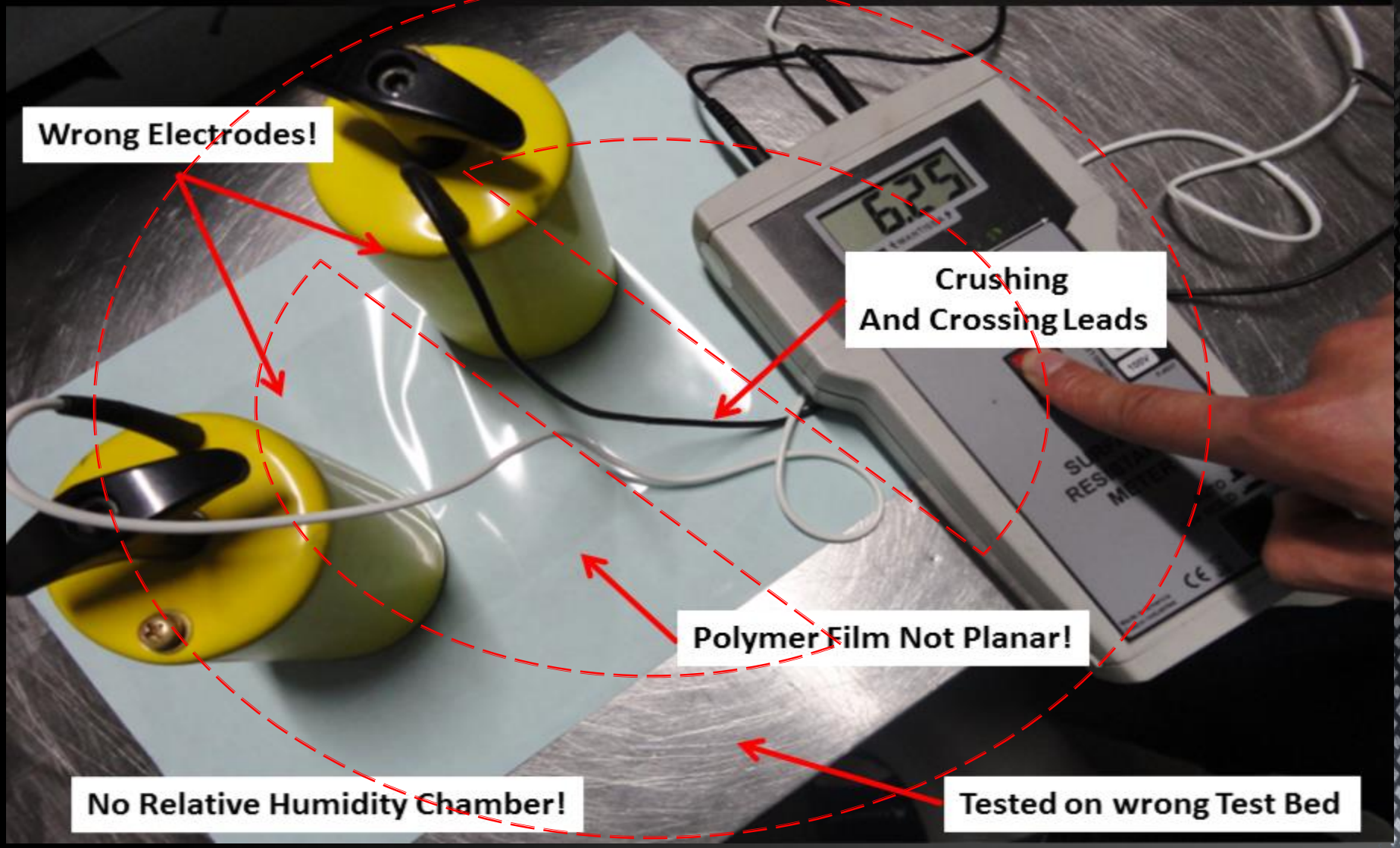
Intel Website

Is ESD Testing Compliant to ANSI/ESD S20.20?

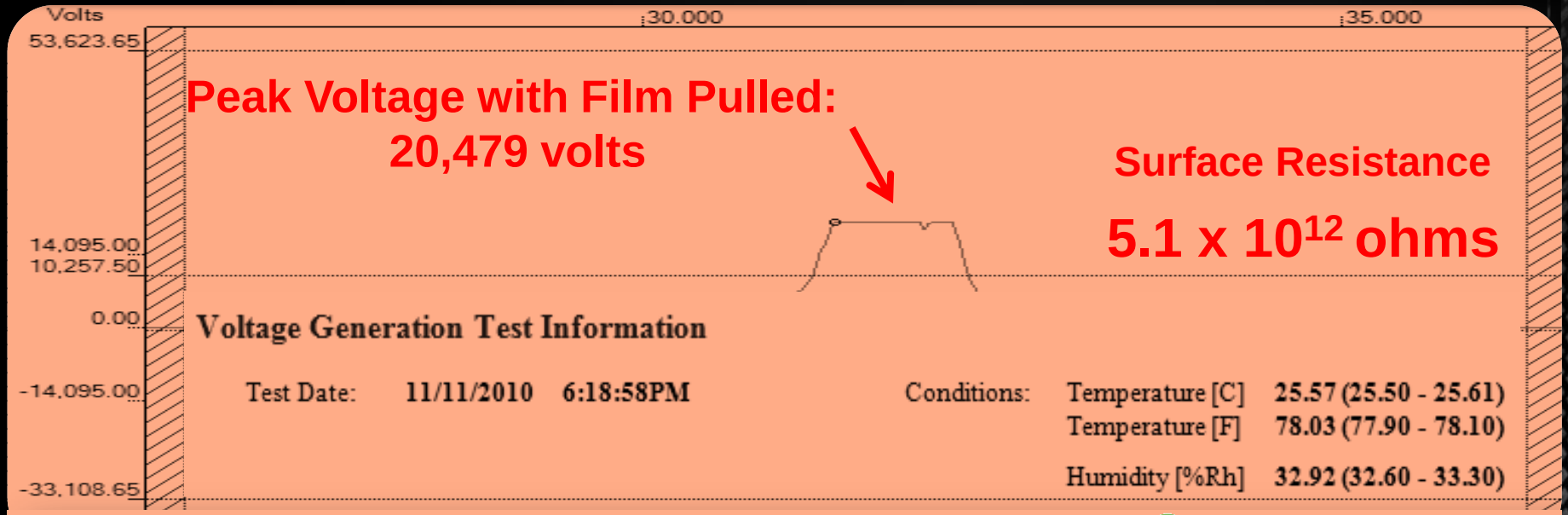
Will a Suspect Counterfeiter Take Shortcuts and make BOGUS Claims?

Touch Screen Display Film

Asian Supplier Bogus Testing Technique for Touch Screen Film Testing Procedures which are not ANSI/ESD STM11.11 Compliant!



How did the Touch Screen Film Test When Pulled?



Voltage Generation Test Information

Test Date: 11/11/2010 6:18:58PM

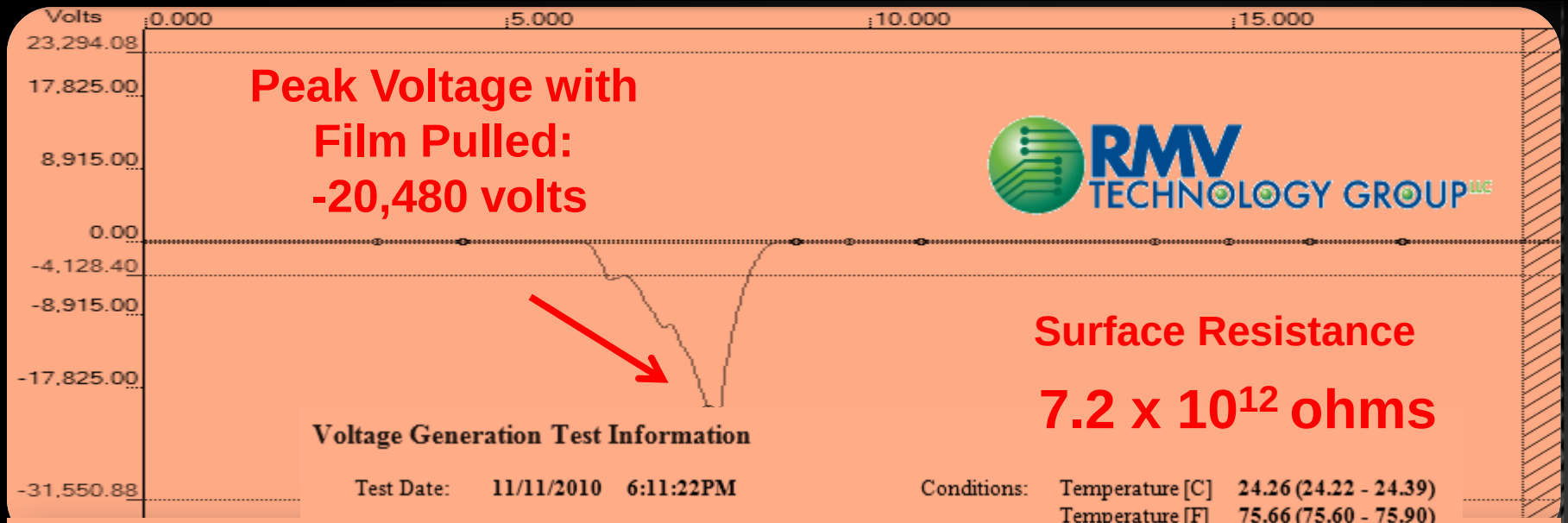
Conditions: Temperature [C] 25.57 (25.50 - 25.61)
Temperature [F] 78.03 (77.90 - 78.10)
Humidity [%Rh] 32.92 (32.60 - 33.30)

Data Summary:

Number of Full Test Cycles: 2

			Min [V] Data	Max [V] Data	Global
		Average Voltage [V]:	-267.00	10,257.50	2,732.80
Peak Recorded Values [V]:	20479.00	Standard Deviation:	100.41	14,455.40	
	-338.00	Minimum Voltage [V]:	-338.00	36.00	-338.00
	-196.00	Maximum Voltage [V]:	-196.00	20,479.00	20,479.00

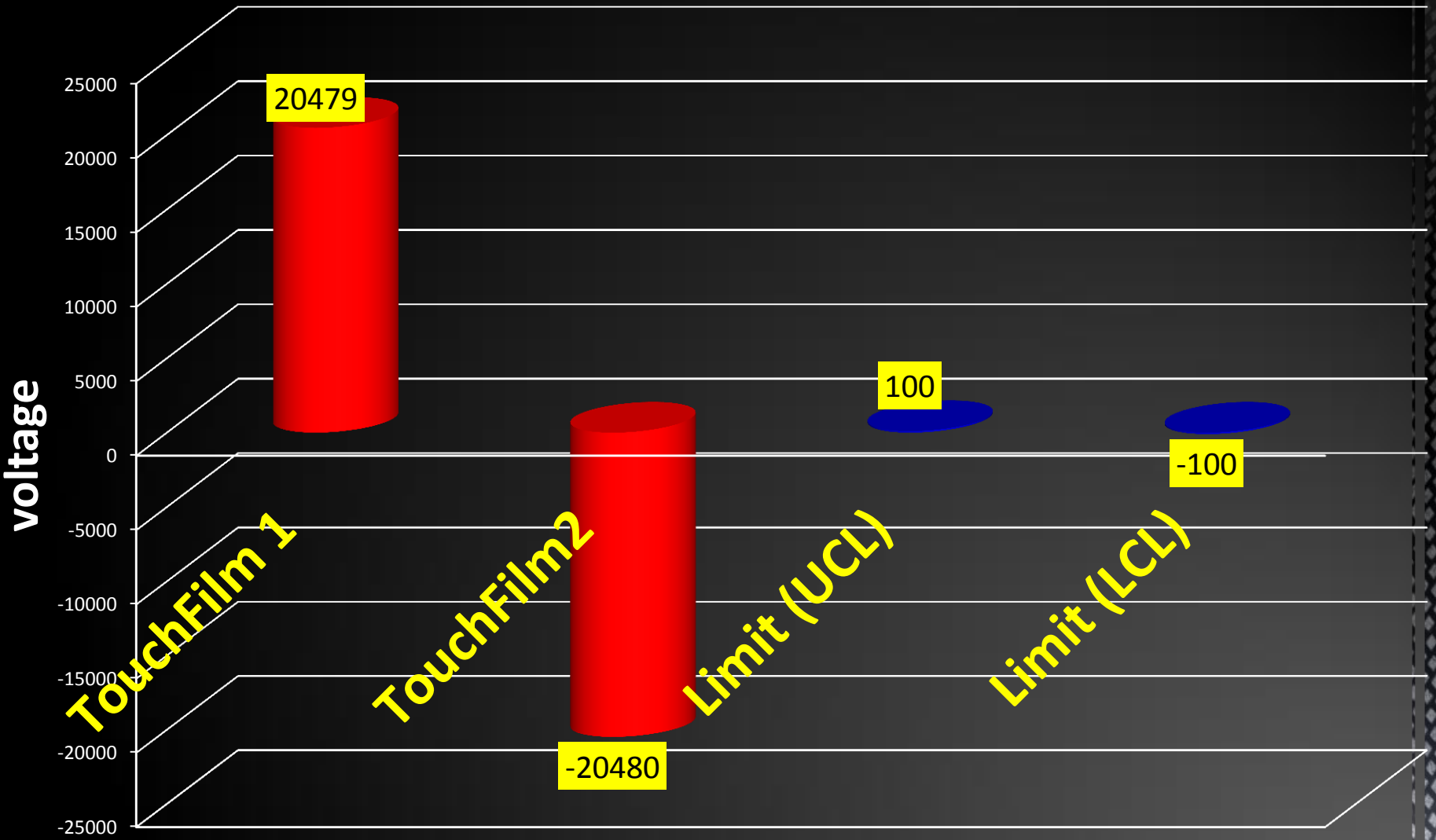
How did the Touch Screen Film Test When Pulled?



Data Summary:

			Min [V] Data	Max [V] Data	Global
Number of Full Test Cycles:	5	Average Voltage [V]:	2.00	-4,128.40	-1,198.95
Peak Recorded Values [V]:	-20480.00	Standard Deviation:	62.45	9,140.83	
	113.00	Minimum Voltage [V]:	-36.00	-20,480.00	-20,480.00
	-51.00	Maximum Voltage [V]:	113.00	-33.00	113.00

Touch Screen Charging at 32%RH



ANSI/ESD STM11.11 Proper Method of Testing

ACIL

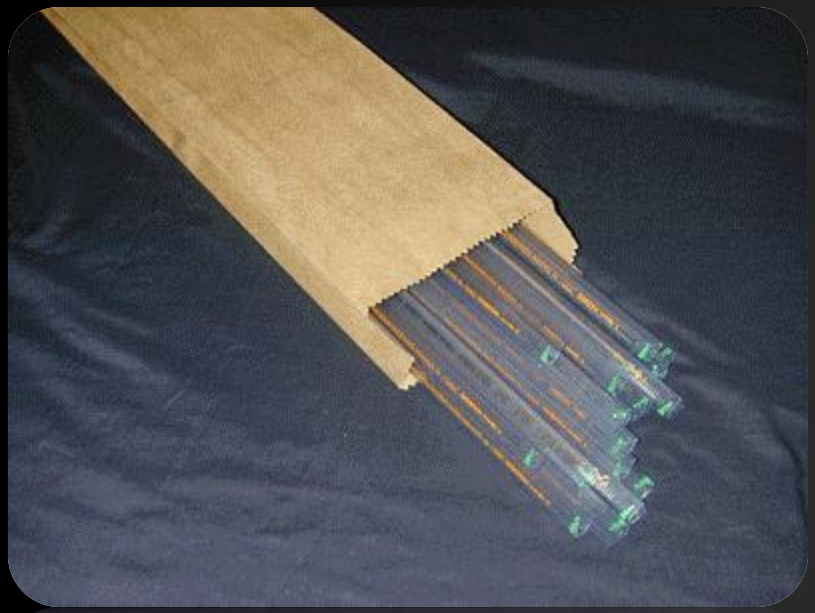
American Council of Independent Laboratories

ENHANCING PUBLIC HEALTH AND SAFETY THROUGH QUALITY TESTING AND ENGINEERING

Mapping ESD Events and Electrostatic Decay

Validate Your Film!

Utilize Proper ESD Practices and Validate before Testing

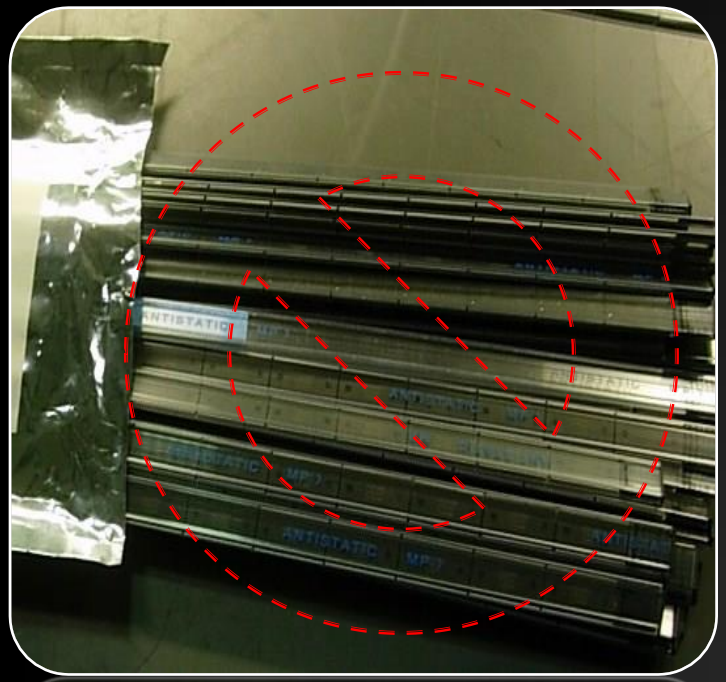


Non-Compliant Dip Tubes Found in Long Term Storage

Issue: User Discovered Insulative Dip Tubes

Fox Guarding the Henhouse
By labsquad

An Aerospace Prime



Quarantined Product

What Happened?

Product placed in Quarantine

What was Found?

Insulative Dip Tubes

What was the resolution?

CM Repacked Tubes

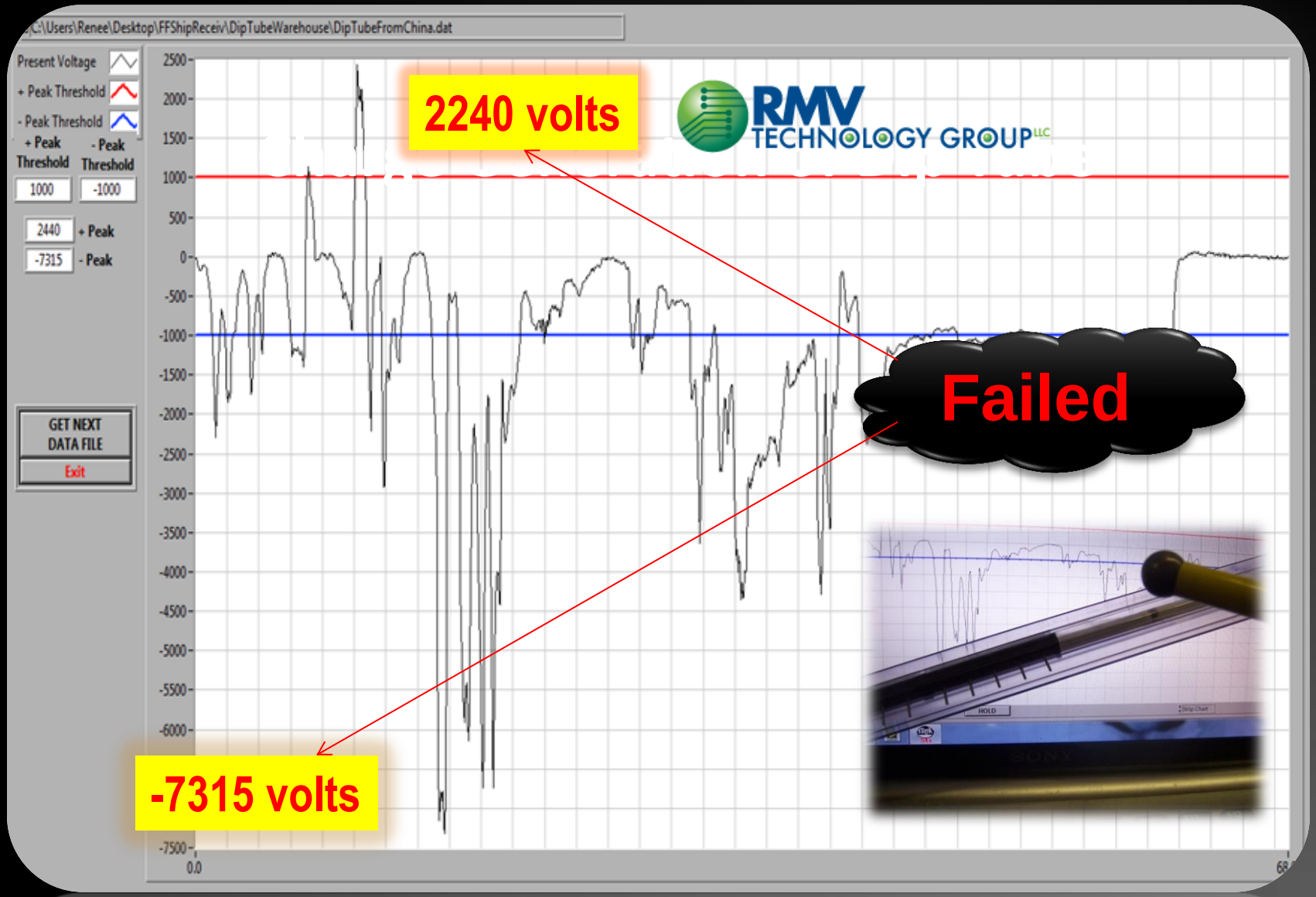
What are the Consequences?

ESD Events during repack can and will take place.

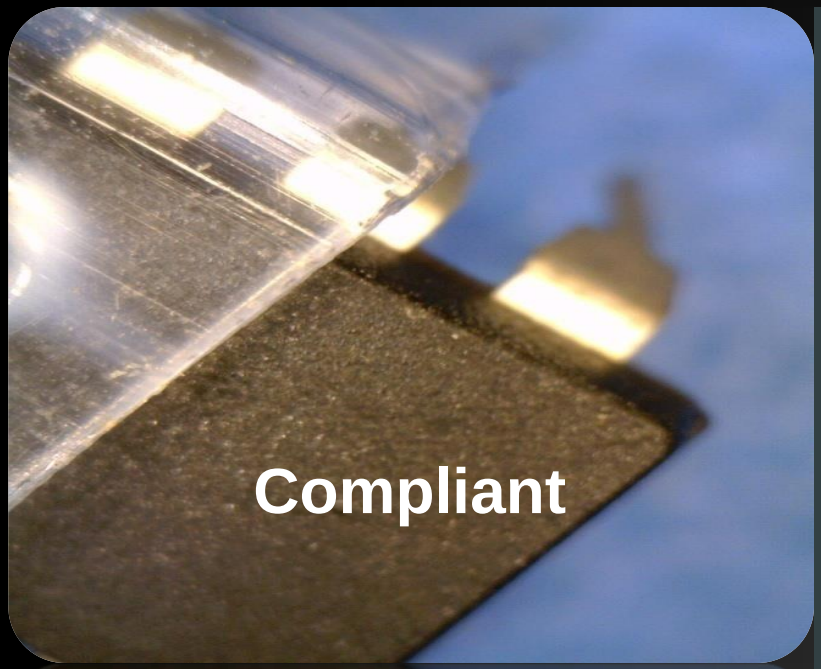
Shock and Vibration during shipment are a cause of FIM Events.

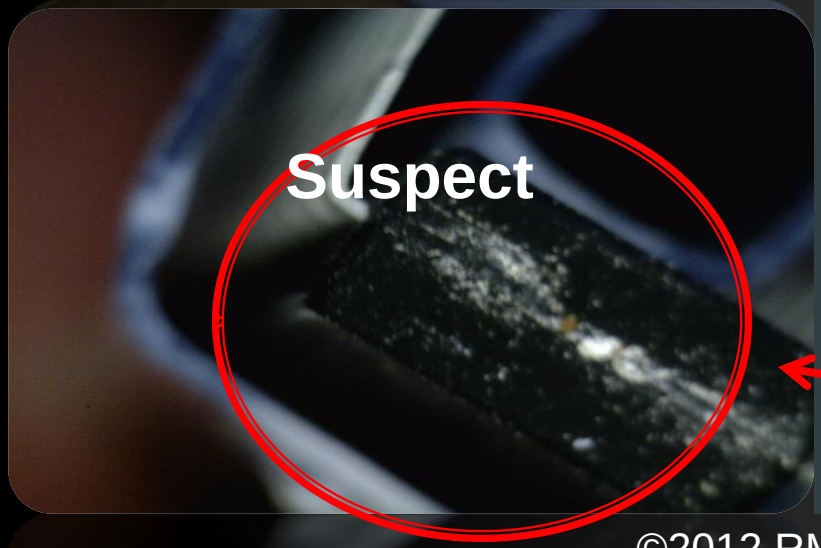
Field Test using 2-Point Resistance of Dip Tube

Suspect Dip Tube Charging at 35%RH



Suspect Counterfeit Risks

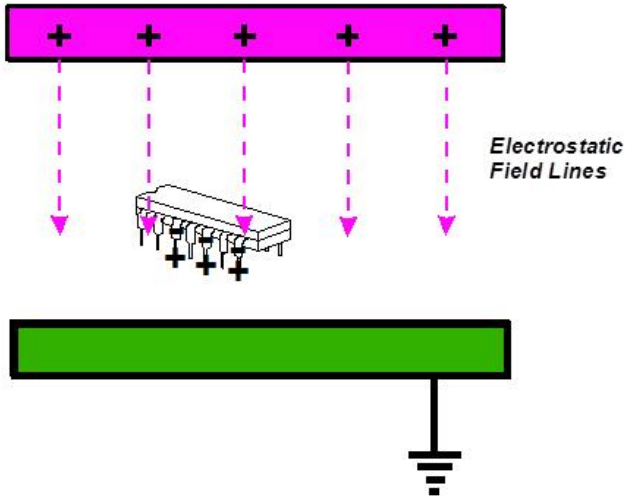


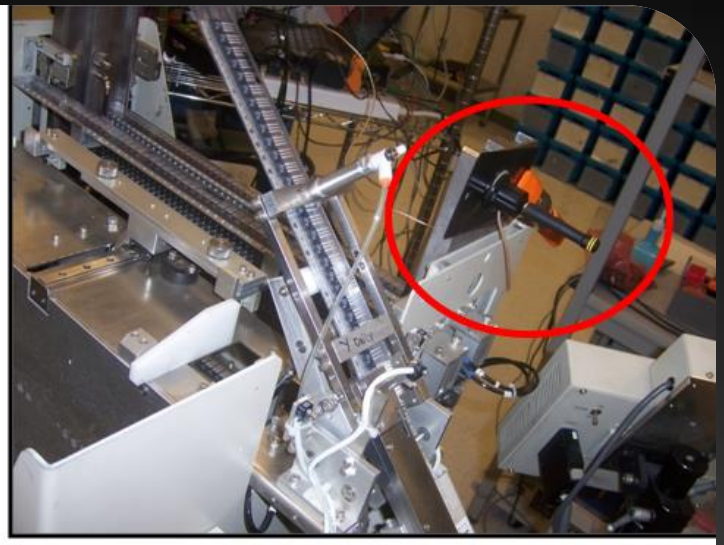


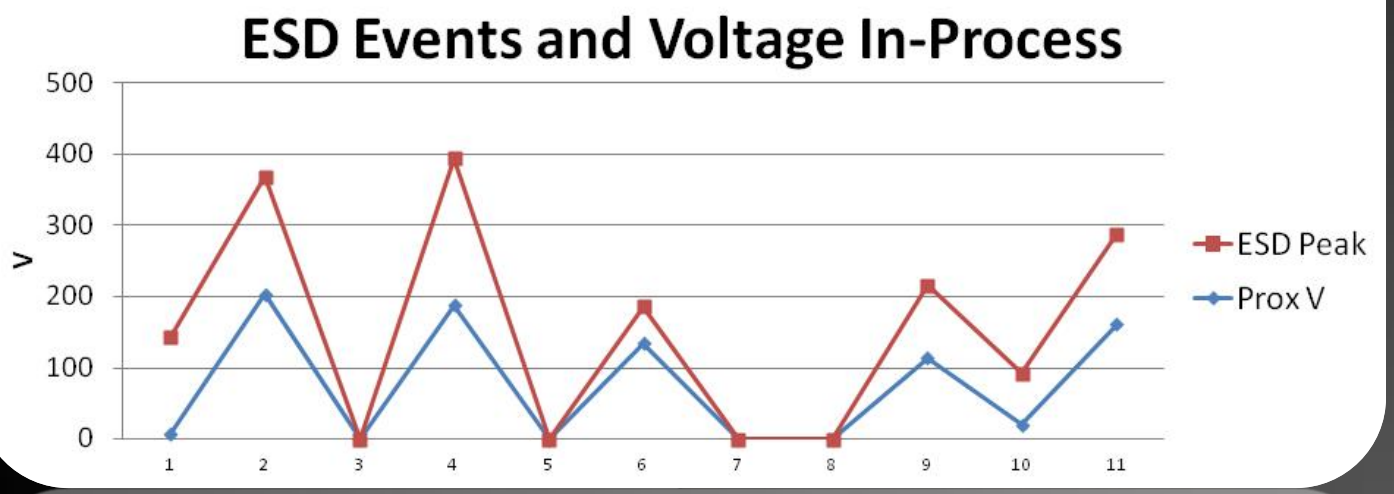
- Recycled Dip Tubes:
  Loss of ESD Properties
- Knock off Dip Tubes:
  Not ESD Safe
- Failures: Handling/Inspection
- Failures: Manufacturing
- Antistatic Migration

Antistatic Transfer

Suspect Dip Tubes = ESD Events







The Cost of Non-Compliance!

What Are the Consequences of Suspect Counterfeit Materials used in Manufacturing, Long Term Storage and Shipping?

According to JPL/NASA Website, ESD Represents a **40 billion dollar** Annual Problem!

- **Tape & Reel Package**

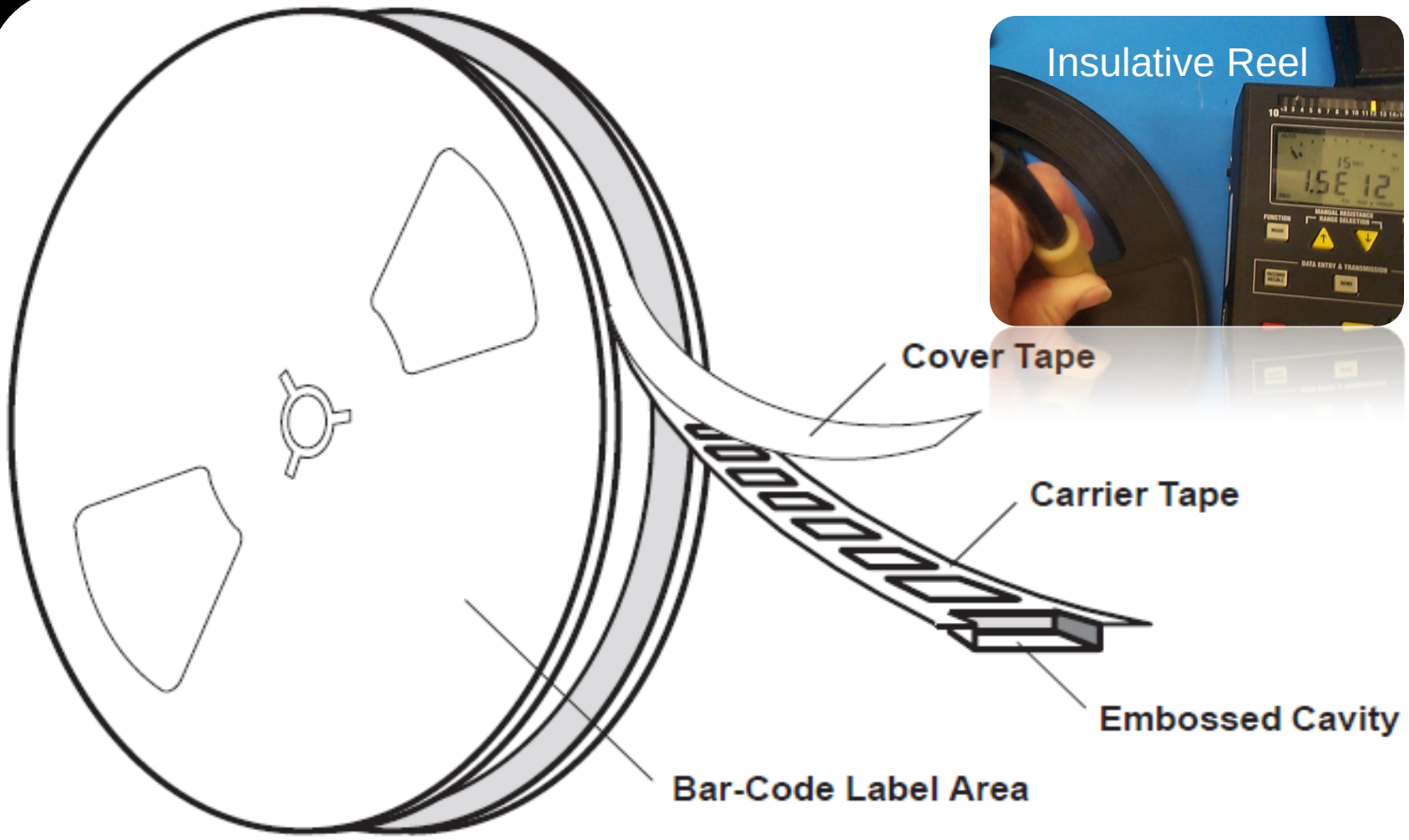
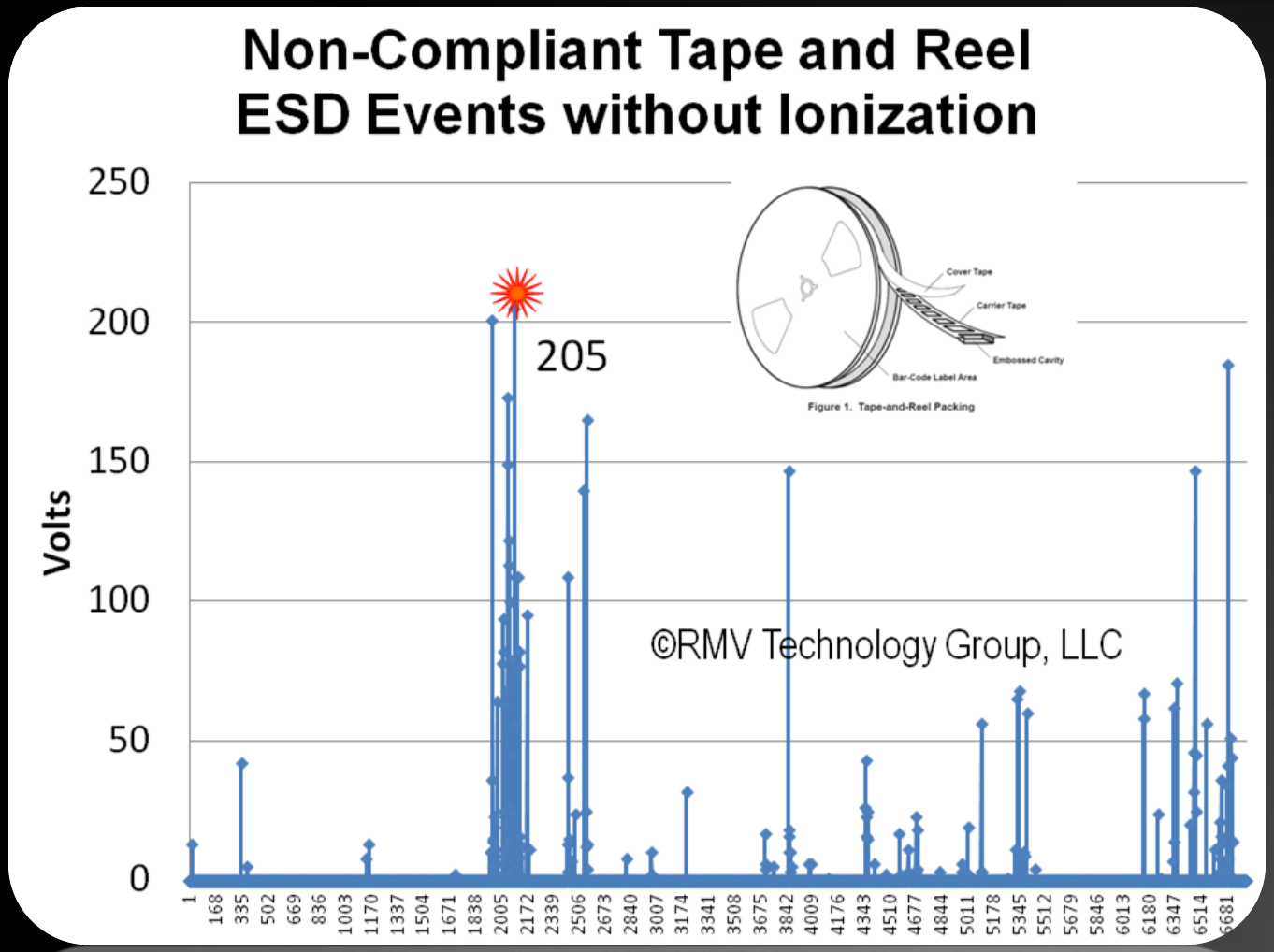


Figure 1. Tape-and-Reel Packing

***"12-mm Tape-and-Reel Component-Delivery System"*, Texas Instruments**

Trust but Verify!

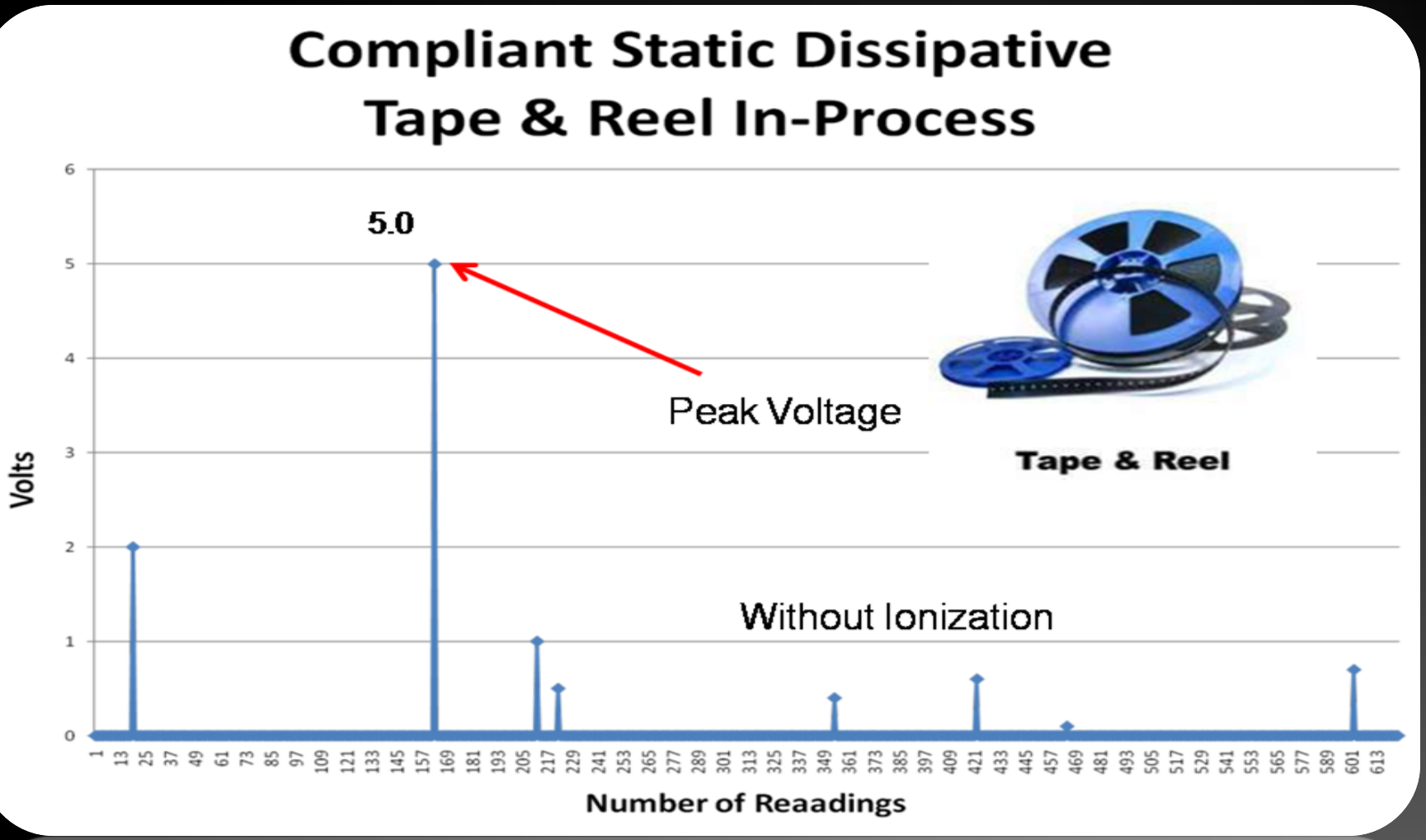
The Risks of Non-Compliance



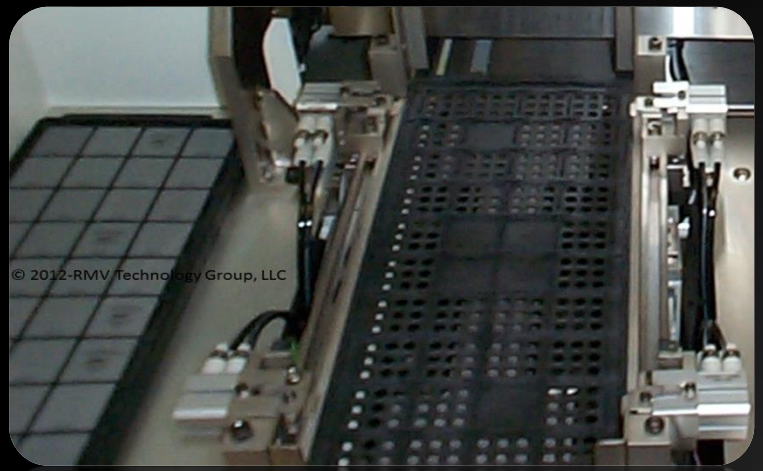
Actual Production Run of Suspect Reel with ESD Components

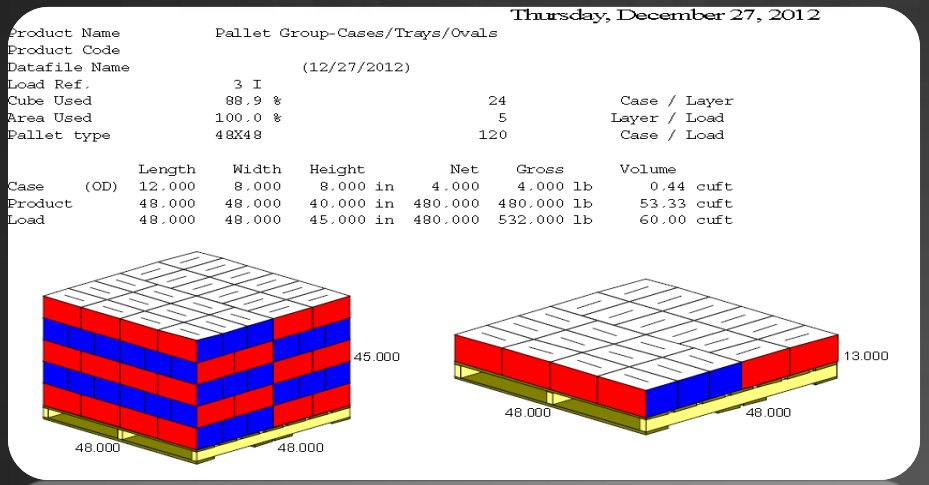
Aerospace & Defense are using <50 volt ESD Sensitive Devices

Compliance = No Failures in Populating a Circuit Card

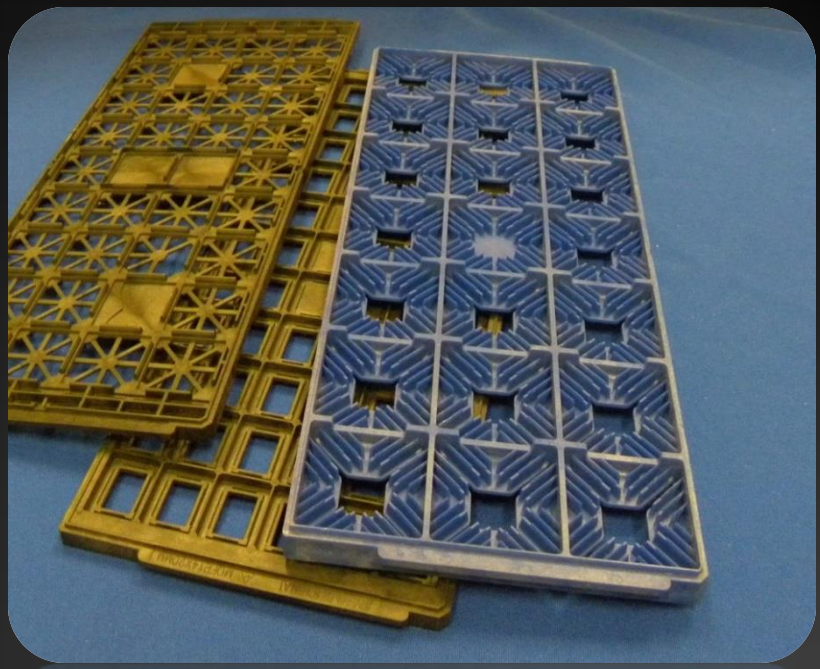


JEDEC Tray, An Overview





JEDEC Tray, An Overview



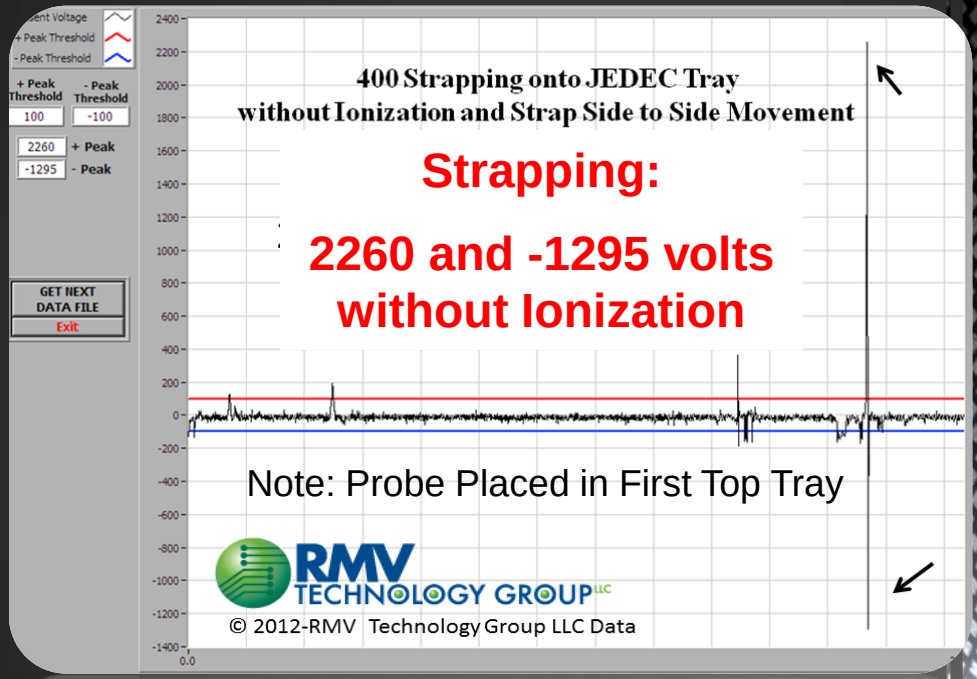
1-Point Resistance through JEDEC on Grounded Surface

BOGUS Trays

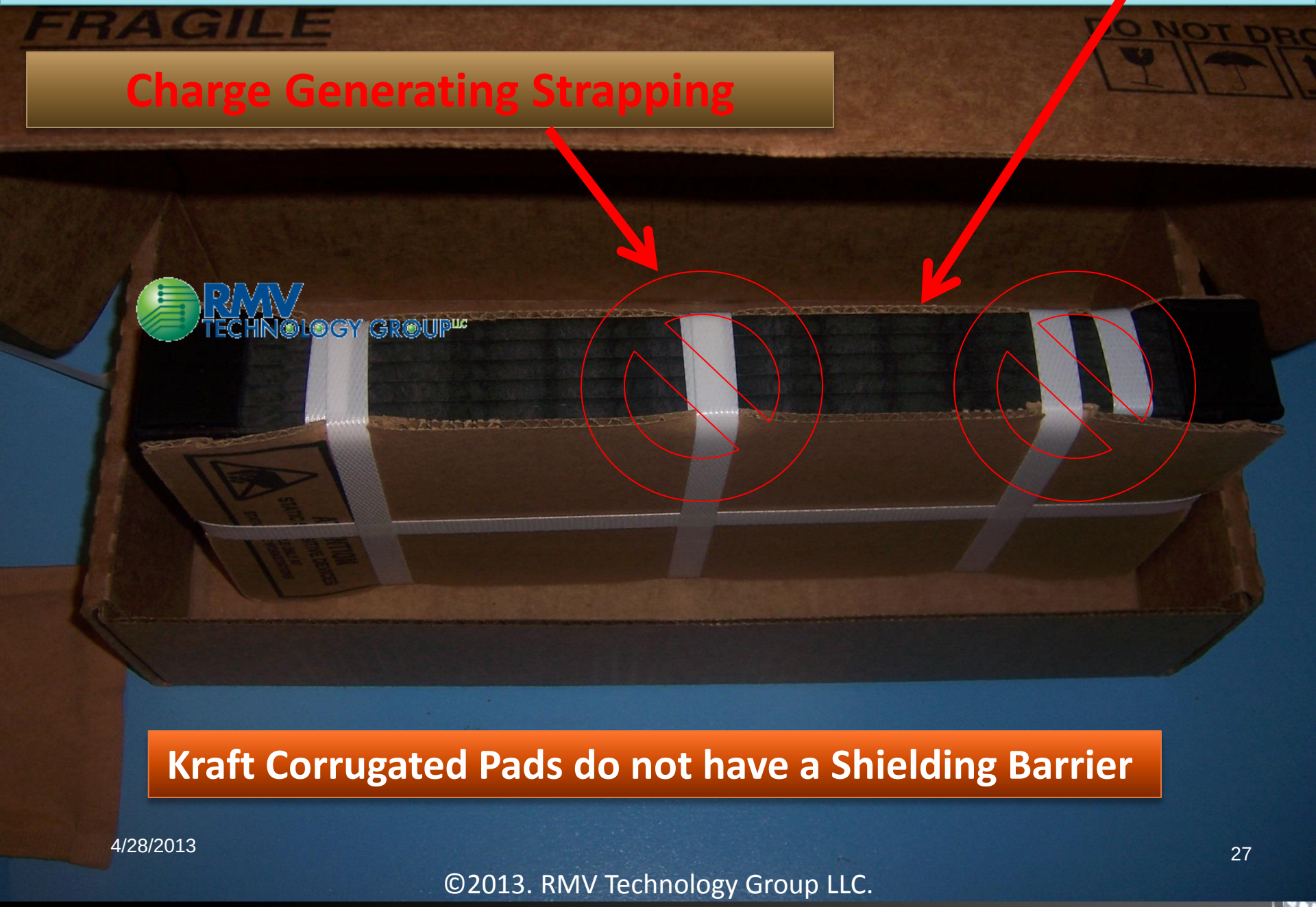
Implementing ANSI/ESD S4.1 & ANSI/ESD S3.1

JEDEC Tray Strapping Charge Generation

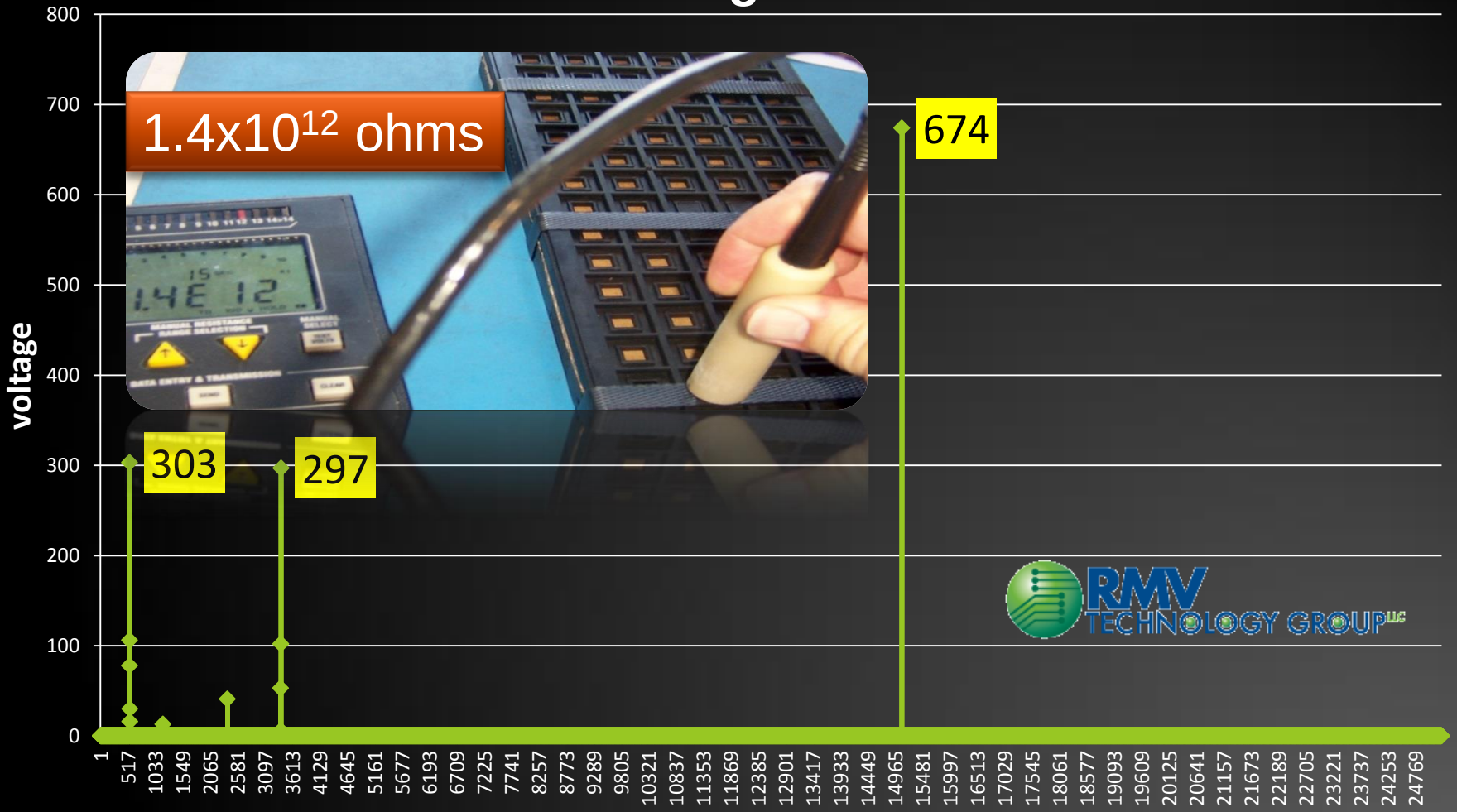
While grounded, conduct the strapping process to stabilize JEDEC tray and contents. Most often, Charge Generating strapping is utilized (a Risk). Therefore, insure the use of shielding top & bottom ESD corrugated cover pads and strapping takes place under high volume velocity air ionization.



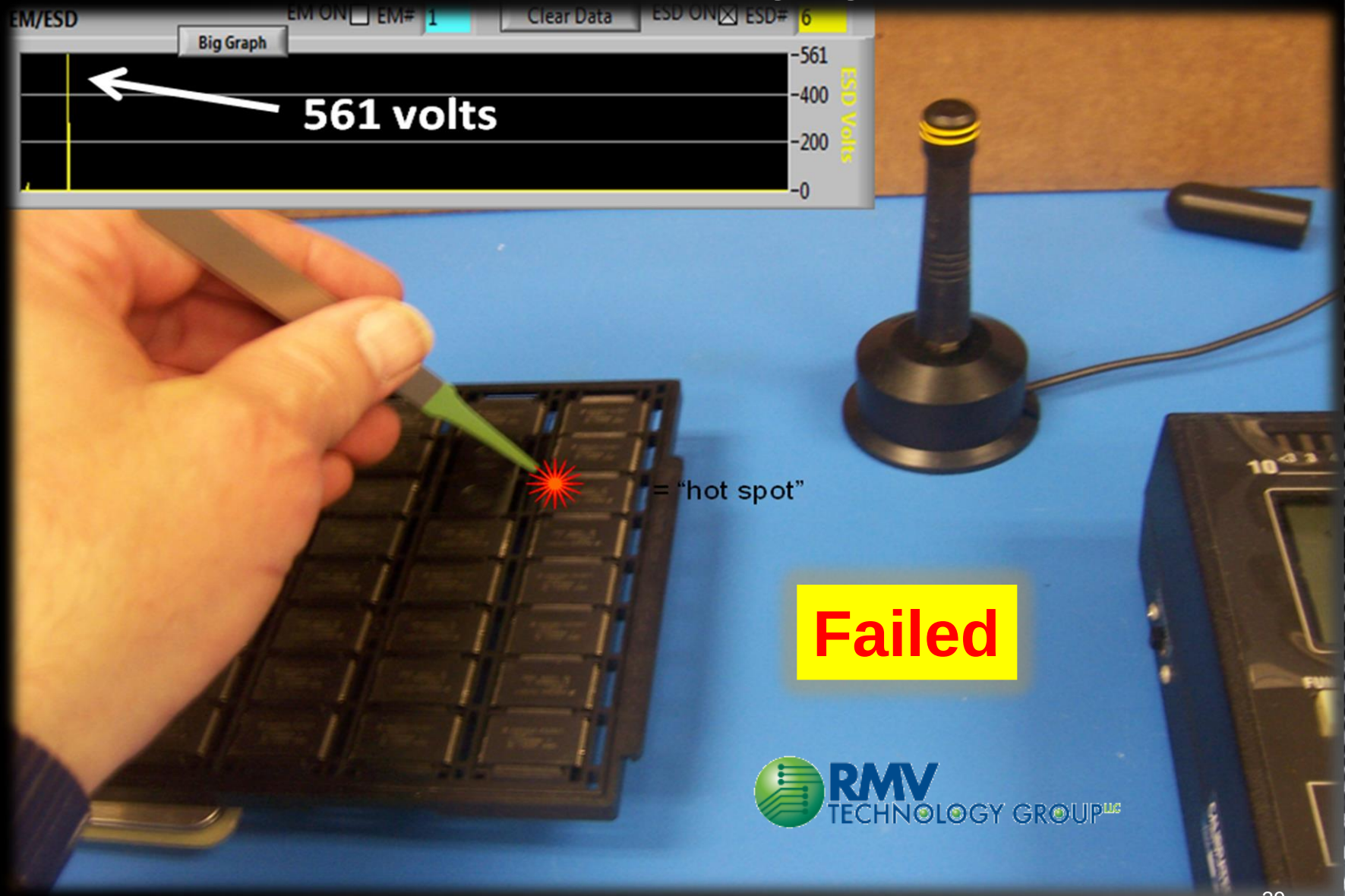
Improper Use of Kraft Corrugated Pads



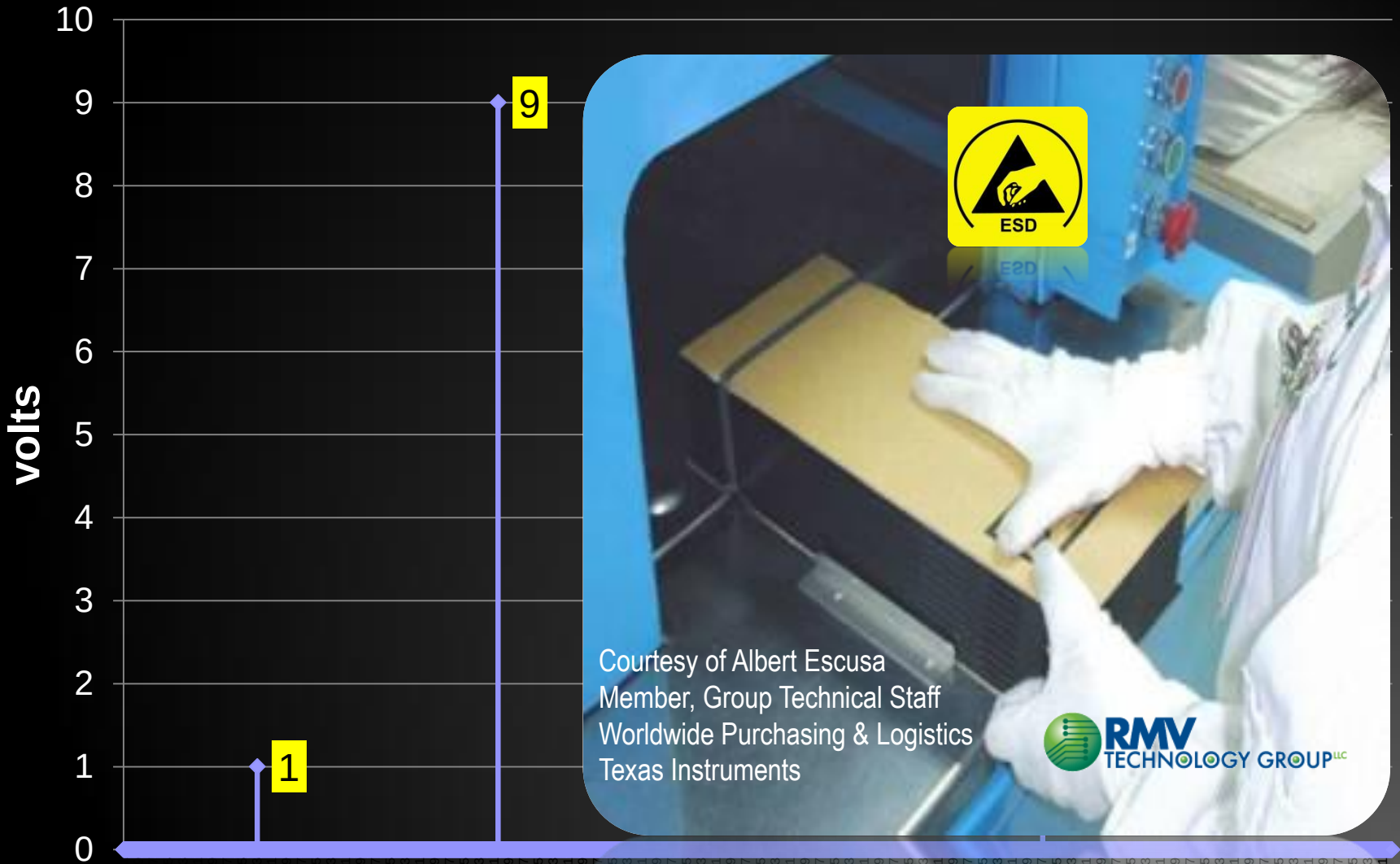
ESD Peak from Nylon Strapping Process into JEDEC Tray without a Conductive Shielding Barrier



Take ESD Precautions During Device Inspection
Be Aware that Counterfeit Packaging is also an Indicator!



ESD Peaks during Strapping Process of JEDEC Tray Using Black Static Dissipative Straps



Texas Instruments ESD Integrity

Black Static Dissipative Strapping!

Recommendations

1. Trust but Verify beyond visual inspection for ESD packaging and materials utilizing ANSI and Mil Standards

2. Traceability to the Country of Origin from Supplier needs to be known as well as using a 3rd party or DoD ESD/Packaging Test Lab

4. All ESD Suppliers Need to Provide CoC per Manufacturer Production Run and require physical ESD testing to Insure compliance

5. Insure DoD Personnel are Properly Trained for ESD Packaging Compliance Including auditors which Need to Take Measurements!

6. ESD Materials Qualification and Verification Testing are Essential!

References

Mil-HDBK-773A, 30June 2005
Nested References:
ANSI/ESD S20.20
ANSI/ESD S541
4.5 U.S. Air Force. U.S. Air Force activities have been instructed to utilize ANSI/ESD S20.20 instead of MIL-STD-1686 and ANSI/ESD S541 instead of MIL-HDBK-263

MIL-DTL-81997D, DETAIL SPECIFICATION: POUCHES, CUSHIONED, FLEXIBLE, ELECTROSTATIC-PROTECTIVE, TRANSPARENT (18-FEB-2004) [SUPERSEDING MIL-P-81997B
Nested References:
Mil-STD-81705
Mil-STD-2073-1

Mil-STD-2073-1E w/Change 1, 7 January 2011
Nested References:
Mil-STD-3010
Mil-PRF-81705

Mil-PRF-81705E X/Amendment 1, 8 February 2010
Nested References:
Mil-STD-3010
ASTM D257
ANSI/ESD STM11.31

NASA MMA-1985-79, Revision 3
23 February 1998
Standard Test Method for Evaluating Triboelectric Charge Generation and Decay

NASA-HANDBOOK 8739.21
This NASA-HANDBOOK is published by NASA to provide standardized guidance for implementing ANSI/ESD S20.20 requirements.
Nested Documents pertaining to packaging:
ANSI/ESD S20.20
ESD TR20.20
ANSI/ESD S541 (includes: ANSI/ESD STM11.11, STM11.12, STM11.13 & STM11.31)

Mil-STD-3010B, Test Method 4046, 31 March 2012
Nested Reference:
Mil-PRF-81705

The Dip Tube

A formalized materials qualification process is essential in preventing non-conforming or suspect counterfeit packaging that can lead to ESD hazards during parts inspection process, long-term storage issues and failures in manufacturing

ROBERT J. VERMILLION, CPP/FELLOW
RMV Technology Group, LLC
NASA Ames Research Park
Moffett Field, CA

The aerospace community has made excellent progress in employing an active defense posture for the inspection of suspect counterfeit parts. From recent industry presentations by the DoD, it does not appear, however, that suspect or non-conforming packaging materials in the supply chain have been considered. Utilization of packaging as a preventative measure in combating the rapid proliferation of counterfeit products will not be addressed in this paper.

The aerospace sector is a relative newcomer to implement anti-counterfeit measures as compared to the medical device and pharmaceutical sectors in the use of packaging engineering countermeasures.

As recently as 2008, the aerospace sector has seen launch delays and issues in space due to non-compliant materials. Since the business model now includes outsourcing with contract manufacturers (CMs) or subcontractors, in-house validation has been replaced by reliance upon the supplier to do the right thing. In addition, reliance upon distribution and supplier driven recommendations is increasing as retirements and layoffs in the aerospace sector continue to accelerate. Consequently, a vendor technical datasheet can prove meaningless unless in-house or third party validation is performed.

To further compound the matter in today's business climate, one is more likely to see Class 0 devices (an ESD sensitive device <250 volts) being incorporated within an ESD controlled aerospace environment. In 1971, the Intel 4004 was equal to about 2300 transistors. Modern day densification has led to a 2 billion transistor equivalency with the Intel® Itanium® processors (codenamed Tukwila) in 2009 up from the previous count of 750,000,000 in 2008. Is aerospace ready for handling ESD sensitive devices less than 50 volts during the inspection and manufacturing process? (See Figure 1).

Do current receiving inspection proto-

CPU Transistor Count 1971 to 2009 (Moore's Law)

→Transistor count

JEDEC and Tape & Reel Issues

Supply chain materials validation for the prevention of non-conforming or suspect counterfeit packaging for in-process manufacturing and long-term storage of Ultra-sensitive (Class 0) ESD devices

ROBERT J. VERMILLION, CPP/Fellow
Certified ESD & Product Safety Engineer
RMV Technology Group, LLC
NASA Ames Research Center (AFC)
Moffett Field, California, USA

Editor's Note: This article is the second part of "The Dip Tube," which appeared in May in the 2010 Interference Technology EMC Directory & Design Guide.

Over the past several years, both European- and U.S.-based organizations have sacrificed the traditional "internal auditing process" with over reliance on offshore contract manufacturers, distributors and suppliers to do the right thing. To compound the problem, organizations will accept supplier specifications as adequate proof in utilizing a product within their supply chain. Since it is now common for organizations to utilize Ultra-sensitive (Class 0) devices at <50 volts (Reference 1), the inspection of Ultra-sensitive (Class 0) ESD susceptible parts is very important. However, without special safeguards, the additional handling to remove and repack the product for validation can cause both physical and ESD damage in the process. For parts, including those that are sensitive to static electricity, measures must be implemented to detect, inspect and validate the packitems have made the news. Three industry sectors are of absolute concern: aerospace & defense, medical device and pharmaceutical drugs.

In this segment, the article will focus on two major packaging types that are utilized to protect Ultra-sensitive devices to and from the distributor by the device manufacturers, then received by the customer for in-process manufacturing.

To the surprise of aerospace and distributor alike, non-compliant or suspect counterfeit conductive or static dissipative JEDEC Trays and antistatic Tape & Reel (T&R) pose real issues during incoming inspection and manufacturing of Ultrasensitive ESD devices. In the May edition of the *Interference Technology 2010 EMC Directory & Design Guide*, non-conformance of antistatic Dip Tube rails was illustrated to compromise compliant ESD sensitive components by using suspect counterfeit, non-conforming or recycled ESD packaging products. Several aerospace engineers stated that this problem had never been considered in developing a Suspect Counterfeit inspection process.

In comparison to the pharmaceutical and medical device sectors, aerospace is a relative newcomer to the implementation of anti-counter-

Interference Technology 2010

http://www.interferencetechnology.com/?s=vermillion&w=a

Contact Us

RMV Technology Group, LLC
NASA Ames Research Center
B 19, Suite 1073, MS 19-46c
Moffett Field, CA 94035-0001
1-650-964-4792

Bob Vermillion, CPP/Fellow
Certified ESD & Product Safety Engineer -iNARTE
CEO/Founder
bob@esdrmv.com
Renee Mitchell, Vice President
renee@esdrmv.com

A Service Disabled Veteran Owned Business, SBA 8(a) & SDB Firm